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THESIS

A PROTOTYPE ENCODING SCHEME FOR ELECTROOPTIC ANALOG TO DIGITAL CONVERTERS

by

Rickey Don Walley

June 1995

Thesis Advisor:	Ron J. Pieper
Co-Advisor:	Phillip E. Pace

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A PROTOTYPE ENCODING SCHEME FOR ELECTROOPTIC ANALOG TO DIGITAL CONVERTERS

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Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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Communications and electronic warfare advances continue to place increasing demands on conventional analog to digital converter designs. This report presents the first experimental prototype system for the use of multiple Mach-Zehnder interferometers as a sampling medium coupled with an electrical encoding scheme based on a symmetrical number system. In addition, a novel error detection scheme is discussed. The new technique provides an improvement in the resolution of electrooptic analog to digital systems beyond the traditional one bit per interferometer and increases the potential bandwidth of these systems to the radio frequency spectrum. The thesis presents the optical bench and electrical design to support this concept and describes a low frequency proof of concept test. Component selection and system alignment procedures are included along with test results and problematic areas.

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I owe a great debt to the American public for an education opportunity that I could not have obtained otherwise and in conclusion I would like to thank my wife and children for their encouragement and support.

I. INTRODUCTION

A. LITERATURE REVIEW

Modern communications and electronic warfare signal processing systems have driven a trend towards moving the analog to digital conversion process into the radio frequency range. This trend coupled with developments in integrated optical fabrication techniques led to research in the use of waveguide electrooptic modulators (Taylor, 1975), (Leonberger, 1979), (King, 1982)) as sampling and encoding systems with resolutions of up to six bits with sampling rates of one Gigasample per second.

These systems shared some common characteristics that are useful in classifying them as a group. The key component(s) of each of these systems was a sampling function that utilized a planar waveguide version of a Mach-Zehnder interferometer. These devices are inherently wideband and can be optically pulsed to perform the sampling function. In each of these systems the resolution was limited to one bit per interferometer. In addition, the systems all used a parallel encoding feature with multiple interferometers with unique bit dependent physical construction (i.e. electrode length).

Recently a technique has been described for extending the range of an integrated optical multi-interferometer analog to digital converter (Pace and Styer, 1994). This method proposed the use of multiple, common, Mach-Zehnder interferometers in a parallel fashion as opposed to the designs which require interferometers with different electrode lengths. A new encoding and error detection method was described based on a Symmetrical Number System which closely emulates the folded wave output of the interferometer. Use of such an encoding would allow extension of the resolution for this system beyond one bit per interferometer.

B. PROPOSED CONCEPT

An analog to digital conversion system is presented based on the encoding of the optical output of three pulsed Mach-Zehnder interferometer devices into a unified digital representation of the original electrical waveform. The input signal is impressed upon the optical system with minor electrical modification for system calibration. The resultant intensity modulated output is detected, amplified and presented to an encoding stage based on a symmetrical number system (SNS) scheme for resolution enhancement. Errors are decimated via the detection and gating of ambiguous states in a simultaneous fashion with the output word encoding.

C. THESIS OUTLINE

Chapter II of this thesis presents background material in support of the electro-optic devices and descriptions of the symmetrical number system encoding technique. General design guidelines, least significant bit calculations and an overview of the error correcting scheme are discussed in Chapter III. Design iterations and optical bench modifications from previous works are described in Chapter IV followed by the as-built performance results of a five bit prototype in Chapter V. An analysis of these results is presented in Chapter VI with conclusion in Chapter VII. Appendices are provided for detailed test methodologies/alignment and firmware documentation.

II. BACKGROUND

A. MACH-ZEHNDER INTERFEROMETER OPTICS

The essential optical component of the electrooptic analog to digital converter is a planar waveguide version of a Mach-Zehnder interferoptic modulator as shown in Figure 1. It consists of an electrooptic crystal (lithium niobate, $LiNbO_3$, for this design) functioning as an planar optical waveguide with electrodes placed on the waveguide for coupling with the applied electrical signal. The crystal is coupled to an optical source via a polarization maintaining fiber optical cable input mated to the optical waveguide via a 3-dB coupler.

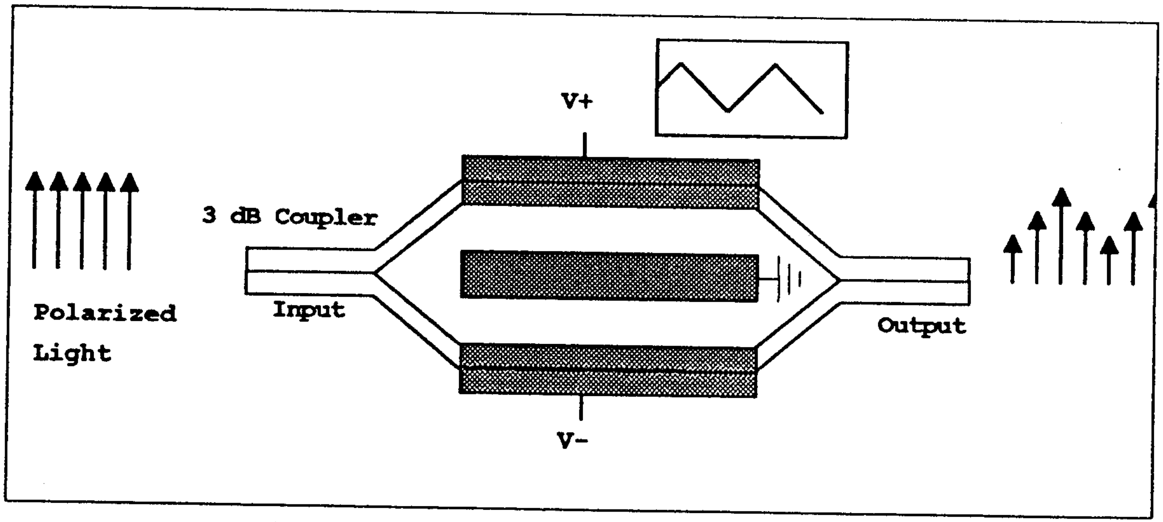


Figure 1. Mach-Zehnder Interferometer Schematic

The input light wave, now divided into equal components, will propagate over the two equal path length arms of the interferometer which are sufficiently separated to prohibit evanescent coupling between them. In the theoretical case if no phase shift is introduced between the interferometer arms, the two components combine in phase at the output 3-dB coupler and continue to propagate undiminished in the output wave guide. If voltage is applied to the electrodes the phase velocity of the light propagating in the arm will be altered due to the linear electrooptic effect (Pockels effect). This will produce a phase difference between the two modulator arms when they recombine, which will reduce the output signal (Alferness, 1982). The minimum output case occurs when the two waves are π radians out of phase. This will result in a null output since the two recombining light waves will try to form a second-order mode which the single mode guide cannot support, and the light will radiate into the substrate (Leonberger, 1979).

The optical output power from a single mode guided-wave interferometer is symmetrical and periodic. The interferometer normalized output as a function of applied voltage can be shown as

$$I = \sin^2(\Delta\phi(v) + \psi). \tag{1}$$

The voltage dependent phase shift $\Delta\phi(v)$ for a push-pull electrode configuration can be expressed in general terms of the electrooptic parameters as

$$\Delta\phi(v) = \frac{2\pi L \Delta n}{\lambda}. \tag{2}$$

where L is the length of the active region in the substrate, Δn is the voltage induced refractive index and λ is the free space optical wavelength. Typically the phase shift ψ is equal to $\pi/2$, however this value may be altered by design or material characteristics to provide an operating point from zero intensity.

Equation 1 can be expressed in terms of a standard Mach-Zehnder parameter V_π

$$I = \sin^2\left(\frac{\pi}{2}\frac{V}{V_\pi} + \Psi\right) \tag{3}$$

where

$$\mathrm{V}_\pi = \frac{\mathrm{G}\lambda}{2\mathrm{L}_i \mathrm{n}_e^3 \mathrm{r}} \tag{4}$$

where n_e is the effective index of the optical guide, Γ is the electrical-optical overlap parameter, L is the length of the electrode for, r is the pertinent electrooptic coefficient, G is the interelectrode gap, and λ is the free-space optical wavelength.

B. SYMMETRICAL NUMBER SYSTEM OVERVIEW

The symmetrical number system is composed of a number of pairwise relatively prime (PRP) moduli m_i. The integers within each symmetrical number system modulus are representative of a symmetrically folded waveform with the period of the waveform equal to twice the PRP modulus. For m given, the integer values within twice the individual modulus are given by

$$x_m = [0, 1, \ldots, m-1, m-1, \ldots, 1, 0]. \qquad (5)$$

The symmetrical number system folding modulus are symmetrical about the midpoint and as such when combined into a multiple moduli system the positional values or states can be used to encode magnitude information of a similarly folded waveform (Pace and Styer, 1994). It is this aspect of the symmetrical number system scheme that complements the output of an electrooptic interferometer. This combination forms the basis for the proposed encoding scheme. Table 1 depicts such a combination of moduli for a modulus 3 and 4 encoder.

Due to the presence of ambiguities, the integers within Equation 5 do not form a complete system of length *2m* by themselves. It is well known however, that the inclusion of additional redundant moduli can effectively detect and correct errors within a residue number system representation of a number. The symmetrical number system formulation is based on a similar concept which allows the ambiguities to occur. The ambiguities that arise within this number system are resolved by using various arrangements of the moduli. By considering the derived moduli arrangements, the symmetrical number system is rendered a complete system having a one-to-one correspondence with the residue number system. In applications such as multiple moduli analog to digital converters the dynamic range *M* of the system is given by Equation 4 where *N* is the number of pairwise relatively prime moduli used in the system

$$M = \prod_{i=1}^{N} m_i . \tag{6}$$

Input index or output state	Modulus 3	Modulus 4
0	0	0
1	1	1
2	2	2
3	2	3
4	1	3
5	0	2
6	0	1
7	1	0
8	2	0
9	2	1
10	1	2
11	0	3
12	0	3
13	1	2

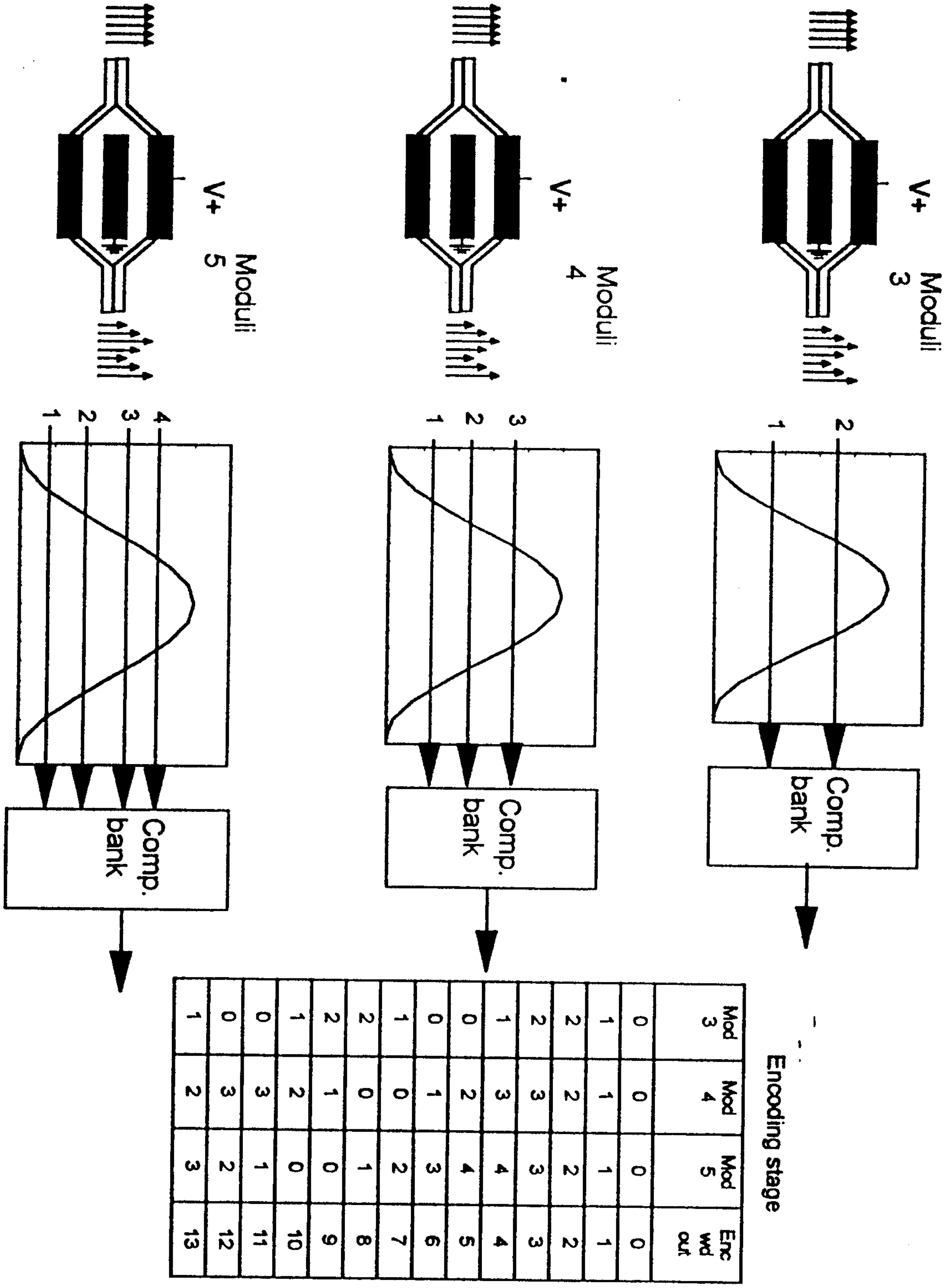
Table 1. SNS System for $m_1=3$ and $m_2=4$

C. INTEFEROMETER/SYMMETRICAL NUMBER SYSTEM INTEGRATION

1. Encoding Scheme

As previously mentioned, the functional similarity between the folding waveforms of an electrooptic interferometer and the symmetrical number system form a unique encoding scheme for analog to digital converters. In previous multiple interferometer based analog to digital converter designs the resolution was limited to one bit per interferometer due to encoding methods (Taylor, 1975), (Leonberger, 1979), (King, 1982). The use of an symmetrical number system can serve as a source for resolution enhancement in an analog to digital converter by decomposing the analog amplitude analyzing function into a number of parallel sub-operations (moduli) that are of smaller computational complexity. Each sub-operation for a different modulus requires only a precision in accordance with that modulus. A much higher resolution is achieved after the results of these low precision sub-operations are recombined. That is, the resolution of each interferometer can be increased beyond one bit per interferometer.

For the proposed method the input signal is folded by a system of parallel Mach-Zehnder interferometers with each folding period equal to twice a particular modulus. The folded waveform at the output of each folding circuit is mid-level quantized with a small comparator ladder to encode the input signal in the symmetrical number system format. An encoder then converts the representation to a more familiar digital output such as a binary representation. With the symmetrical number system encoding any combination of folding periods and comparator arrangements can be analyzed exactly. Figure 2 depicts such a proposed system.



Mod 3	Mod 4	Mod 5	Enc wd out
0	0	0	0
1	1	1	1
2	2	2	2
2	3	3	3
1	3	4	4
0	2	4	5
0	1	3	6
1	0	2	7
2	0	1	8
2	1	0	9
1	2	0	10
0	3	1	11
0	3	2	12
1	2	3	13

Figure 2. Proposed MZI/SNS Encoding

2. Sampling Pulse Requirements

As with any analog to digital conversion scheme, the sampling criteria is dependent upon the capability of the sampling system and the maximum intended input frequency. In typical applications the optical interferometer is used in a continuous fashion to modulate a signal for coupling into an optical fiber. A benefit of the Mach-Zehnder interferometer construction is in the possible dual use of the device as a very high speed switch. When combined with high bandwidth electrical input characteristics a powerful sampling function can be developed.

Pace and Styer (1994) determined the sampling pulse width requirements via an analysis of error in the sampled input voltage due to the total electrooptical interaction time (or laser pulse width) ΔT. The results of this analysis led to a derivation of a pulse width limitation as shown by

$$\Delta T < \frac{\sqrt{\frac{3}{2^{B-1}}}}{\pi f_{\max}} \tag{7}$$

where B is the bit resolution and f_{max} is the maximum input frequency.

A plot of resolution vs. pulse width and maximum input frequency for systems under consideration is shown in Figure 3. In addition to the pulse width requirements Nyquist criteria must be considered for the sample pulse repetition interval. In all cases considered for this thesis a minimum of twice the sampled frequency will be assumed.

Pulse width and interval timing variations must also be considered in sampling analog to digital systems. These variations or "jitter" baseline the accuracy of the conversion process. In a similar analysis to equation 5 the maximum allowable deviation ($\delta t_{\max}$) based on resolution and maximum input frequency is (Pace,1994)

$$\delta t_{\max} < \frac{1}{2^{B+1}\pi f_{\max}}. \tag{8}$$

For example, a five bit system designed for a 2.5 MHz maximum input should have a pulse source with less than 2 nsec jitter. While this is a readily available stability criteria, significant increases in the input frequency proportionally increase the jitter requirements into areas beyond the capabilities of silicon based systems. Electrooptical systems have an alternative method for pulse generation in mode locked laser systems for picosecond or better resolutions.

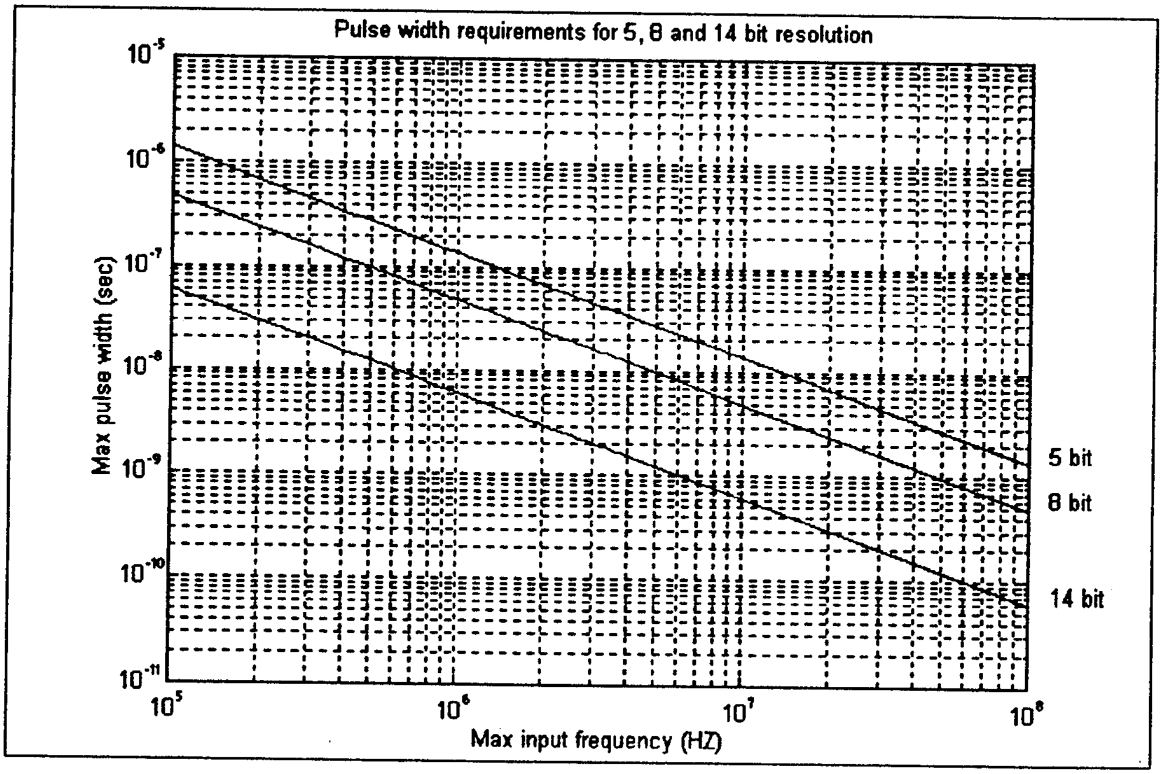


Figure 3. Pulse Width Requirements

III. MZI-SNS BASED SYSTEM DESIGN GUIDELINES

A. DESIGN PARAMETERS

The proposed analog to digital conversion system employs integrated optical interferometers to preprocess the analog signal. Each interferometer folds the input signal at a particular pair wise relatively prime modulus m_i and a small comparator ladder is used after each detector to detect the various voltage levels and encode the input signal into the symmetrical number system format. To facilitate this process there are two key parameters in the choice or design of the interferometer, V_π and V_{max}. The first performance specification is the amount of electrode voltage needed to transition the normalized output from a minimum ($\Delta\phi=0$) to a maximum ($\Delta\phi=\pi$) or V_π. The second specification is V_{max} or the maximum allowed voltage before a dielectric breakdown occurs in the electrooptic crystal/electrode structure (Pace, 1995).

The optical output power from a single guided-wave inteferometer is symmetrical and periodic and can thus be used to implement each folding circuit (modulus) in the symmetrical number system analog to digital converter. The interferometer normalized output is a function of both the sampled analog voltage V and the modulus m_i as

$$I(v_i) = \sin^2(\tfrac{\pi v_i}{2V_\pi}),\ i \in \{1,2,\cdots,N\} \tag{9}$$

where v_i is the modulus dependent attenuated input signal. The attenuation factor depends on the modulus in such a was that identical interferometers can be used. Specifically, we can take

$$v_i = \tfrac{m_{\min}}{m_i}V \leq V \tag{10}$$

where V is the input signal. V_π is the half wave voltage for the MZI. m_{min} is the minimum modulus of the set needed to satisfy Equation 6.

The folding circuit for each modulus requires m_i-*1* comparators at the output of the detector. With the waveform given by Equation 9, the normalized threshold values for the comparators within each modulus m_i are

$$T_{i,j} = \sin^2\left(\frac{\pi}{2}\frac{v_j}{V_\pi}\right) \tag{11}$$

where

$$v_j = \frac{j}{m_i}V_\pi \quad j \in \{1, 2, \cdots, m_i - 1\}. \tag{12}$$

That is , the comparator thresholds are tailored to the interferometer output waveform.

The specifications of V_π and V_{max} reveal the maximum number of folds available from the device. A complete fold is a period formed by application of $2V_\pi$. Therefore maximum number of folds *F* available from a device is

$$F = \frac{2V_{max}}{2V_\pi}. \tag{13}$$

The smallest modulus within the symmetrical number system requires the largest number of folds to instrument the dynamic range *M*. Since a complete fold is $2V_\pi$ and in the encoding scheme this is equivalent to twice the modulus folding period or $2m_i$, the largest number of folds required from an interferometer in a *B*-bit symmetrical number system analog to digital converter is

$$F_{req} = \frac{2^B - 1}{2m_{min}} < \frac{V_{max}}{V_\pi}, \tag{14}$$

where m_{min} is the smallest modulus in the SNS system.

Consideration must also be given to the relationship between the dynamic range of the moduli M, as expressed in Equation 1 and the resolution of final stage of encoding B. The desired resolution should satisfy the expression

$$M \geq 2^B \tag{15}$$

B. LEAST SIGNIFICANT BIT DETERMINATION

One of the most common specification of a generic analog to digital conversion system is the least significant bit (LSB). This parameter represents the smallest quantized value of input resolved at the output word of the converter. For an Mach-Zehnder interferometer based analog to digital system, the least significant bit can be determined by dividing the interferometers V_π voltage by the minimum modulus for the system as shown in Equation 16. For example, a five bit system with a V_π of 2.2 volts and a minimum modulus of 3 has an LSB of 0.73 volts.

$$V_{LSB} = \frac{V\pi}{m_{min}} \tag{16}$$

C. ERROR DETECTION

In symmetrical. number system based analog to digital converters, the folding waveforms and comparator levels together divide the input voltage into M regions of equal size. The points at which the folding waveforms cross the comparator thresholds all occur at the same input voltage. The symmetrical. number system can present a problem at each of these specific voltage levels. The threshold levels need to be crossed simultaneously for all of the moduli. When some comparators, at a position to change, do change, while others do not, the recovered amplitude will have a large error. The probability of this occurrence depends on the offset voltage match of the comparators, the tolerance of the voltage dividing resistors and the corresponding width of the input voltage region being affected. In other words, we can accept the fact that a small portion of the sampled voltage levels will fall in this critical range and give false amplitudes.

The other alternative is to discard the errors using a few additional comparators. On the least modulus, m_1, we use $2m_i$ comparators rather than m_i-1. Of these, $2m_i$-2 would be paired, one just below the comparator threshold and the other just above. Of the other two, one would be just above the minimum modulation depth, and the other threshold just below the maximum detector output. Let us assume that a signal arrives and all comparators below a certain level are on. This is as it should be. For each incoming signal, if it turns out that an *even* number of comparators, 0, 2, 4, ..., $2m_i$, the signal is rejected. If it turns on an *odd* number of comparators, it is accepted. In this manner a narrow window is placed around each voltage that corresponds to a switching point. For all other moduli, the comparators levels are adjusted so that they fall within these narrow bands. Any input signal within these narrow rejection bands can be easily discarded. Figure 4 qualitatively depicts the comparator bands for error detection across a "simplified" modulus 4 waveform. In actuality, the waveform is not linear but follows the dependence given in Equation 8. Similarly, the spacing between the error bands would not be linear.

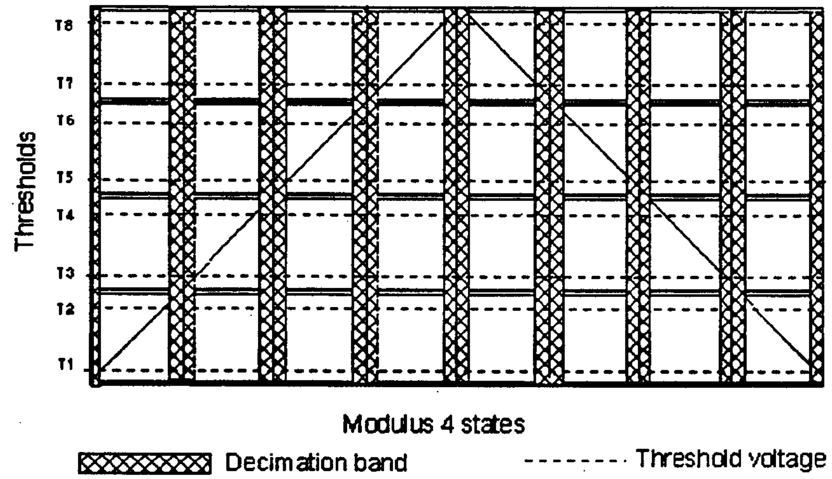


Figure 4. Decimation Bands for Error Detection

D. PROPOSED SYSTEM

The electrooptic analog to digital converter design proposed is based on the concept of a encoding the input signal via a combination of multiple interferometer generated samples. These discrete samples are digitally sampled and the unique combination is interpreted into a resultant output state. A block diagram of a single channel of the system (representing the minimum modulus) is presented in Figure 5.

As shown, the initial stage of the system is the laser pulse generation. It is essential at this stage to also recognize one of the key requirements for the optical pulse input to the Mach-Zehnder interferometer, linear polarization. It is typical of lasing systems, especially commercial grade communications lasers, to be polarized however most manufacturers do not specify this or determine the polarization mode for user mechanical keying purposes. At this juncture the user must decide whether to use polarization maintaining fiber for the input (and accept the inherent cost and technical problems of keying for the correct mode) or use a short span of single mode fiber and use a fiber coupler with a keying system that can be rotated, the latter has been chosen with some success in this project. The output of the interferometer is not polarization sensitive it is a combination of the polarization modes in each arm after electrooptic rotation and hence may be coupled to the photodetector via single mode optical fiber.

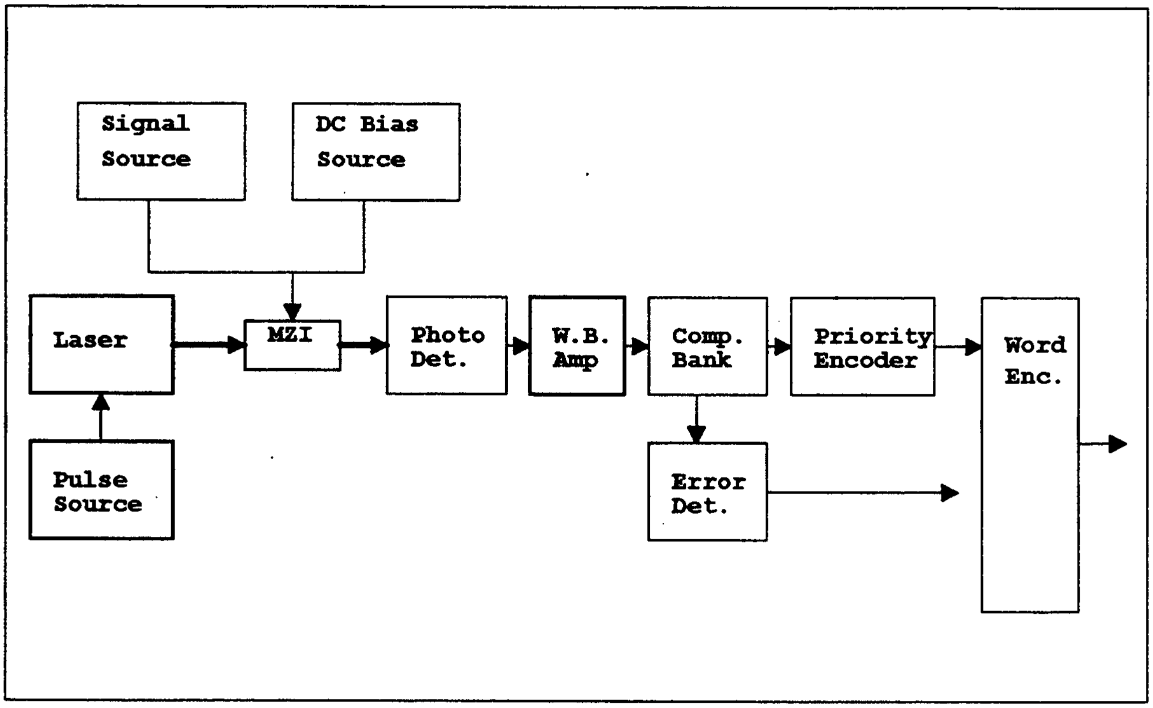


Figure 5. Single Channel System Block Diagram

The input signal is coupled to the interferometer electrodes via a gain stage that facilitates an electrical attenuation relative to the minimum modulus. This design provides for the use of a standard interferoptic device for a multiple interferometer system vice custom length devices designed for a specific modulus. The DC bias function is necessary for the alignment of the folding waveforms to a common phase point for initialization of the "one-up" output word encoding method. It should be noted that in most applications this DC bias should be applied as offset to the input of the wideband amplification stage so as to not distort the amplified signal input.

After the optical pulse has been modulated by the Mach-Zehnder interferometer, the intensity is converted to an viable electrical pulse by a photodetector and another wideband amplifier stage. The required amplification is determined by a combination of factors such as optical power coupled to the photodetector, the photodetector sensitivity and comparator input full scale voltage. The gain should be such that the comparator bank voltage reference is matched and the comparators are not overdriven.

The comparator bank resolves the electrical pulse into a magnitude represented by the number of comparators set to the enabled state, sometimes referred to as a "thermometer code." The comparator bank output is then encoded into a binary representation (with number of parallel lines dependent upon the size of the comparator bank) by the logical priority encoder function. The priority encoder function represents the last stage where a unique representation of a given modulus is available.

The final output word can be formed in a number of fashions. This block is normally represented by a Programmable Logic Array or other memory function without detail. This function has been practically implemented for slow speed designs with Erasable Programmable Read Only Memories (EPROM) and in lower resolution systems with Generic Array Logic (GAL) devices.

The final stage for discussion is the Error Detection Function. This can be implemented via a standard parity encoder logic function since the goal is to determine whether an even or odd number of comparators are enabled. Standard Medium Scale Integration devices of sufficient speed are available for low resolution designs, or GAL devices may be used for higher resolution devices.

IV. DESIGN GOALS

A. INITIAL DESIGN GOAL

The design goal for this phase of the EO-ADC project was to produce a intermediate capability eight bit prototype converter based on the usage of three MZI on loan from other national research facilities. With the use of existing optical devices and resolution as a constraint, the system was reverse engineered from the characteristics of the interferometers. The optical bench for this phase of the project is shown as Figure 6, this design was initially designed and described by Crowe (1995).

The basic parameters of the loaned MZI were described by NRL and Crowe (1995). From Equation 13 and a typical value for V_π of 2.25 volts and a V_{max} of approximately 30 volts, the maximum integer number of folds was 15. Equation 14 limits the system to minimum modulus of 9 with a resulting choice of moduli 10 and 11 to satisfy the dynamic range vs resolution requirements shown in Equation 15.

Timing requirements for the system are defined by Nyquist criteria for sampling rate (or pulse repetition interval), Equation 7 for maximum pulse width and Equation 8 for pulse jitter. An ambitious goal of a 5 megasamples per second (Msps) was decided upon thus allowing a maximum input frequency of 2.5 MHz. For this set of parameters a 20 nsec optical pulse width was chosen. A derived result of this selection was also the conversion time for the system components. If a 5 nsec propagation delay for optical path and electrical gain stages is chosen this leads to a maximum encoding stage propagation delay of 175 nsec.

Modifications to the optical bench were required in order to minimize pulse jitter while allowing for variations in the system parameters for test purposes. The system as described by Crowe (1995) was adequate for characterization of the MZI but was a continuously variable adjustment for the pulse characteristics vice a discrete step system. Such a discrete system was deemed necessary for repeatable testing and will be discussed in Chapter IV.

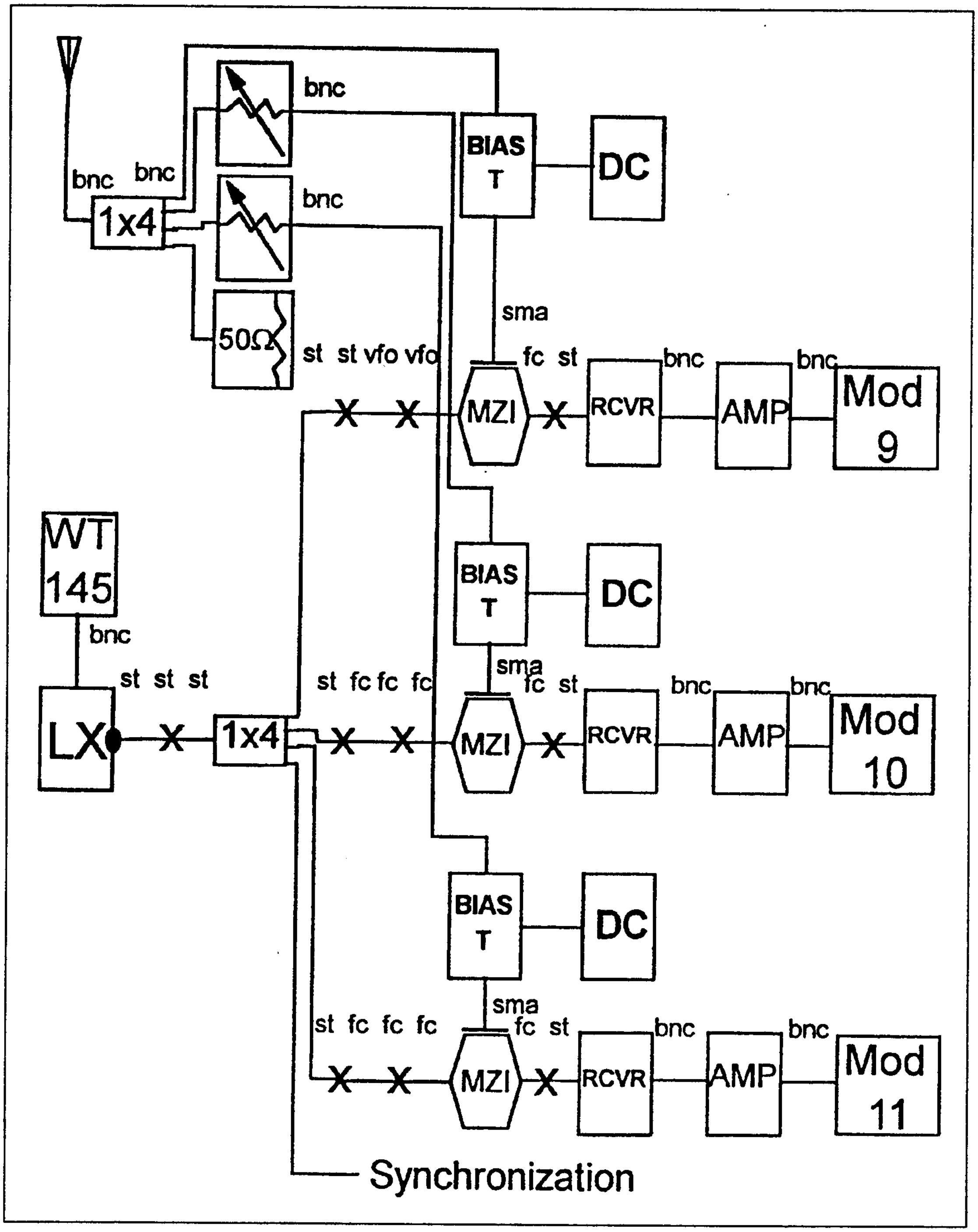


Figure 6. Initial Optical Bench (Crowe, 1995)

In conjunction with the stated design goals it was decided to not use an intermediate sample and hold function at the comparator bank stage. A combinational asynchronous logic format was chosen up to a final output data latch. These constraints were accepted to avoid further timing limitations on the sampling and encoding circuits and allow the use of the laser pulse for system synchronization.

Emphasis was also placed on using only readily available parts vice the inherent costs and risks of custom integrated circuits. Transistor-Transistor Logic (TTL) was chosen as the logic family of choice for this phase due to the wide availability of programmable logic devices in this family. Wire-wrap techniques were to be used through out the design to expedite modifications and minimize costs.

In the optical path, single mode (SM) optical fiber was used whenever possible vice polarization maintaining (PM) fiber due to cost and a lack of proper alignment capability for PM fiber. This was a concern and possible error modes will be discussed in later chapters. The decision for single mode fiber led to the use of special panel mounts for the interface with polarization maintaining fiber that allowed for rotation of the connector keying mechanism thus allowing for a close match for polarization.

B. MACH-ZEHNDER LIMITATIONS

During testing of the interferometers used in this prototype it was noticed that the devices exhibited a non-uniform extinction ratio characteristic when swept across the extremes of the intended operating range (+/- 30 V). Figure 7 is shown as an example of this deviation across the +/- 30 volt range. This was determined to be unacceptable for the eight bit design. However it was found that the interferometers performed in a more uniform fashion when the input voltage was limited to approximately +/- 12 volts. This was accepted as the best compromise and a new set of design parameters were chosen.

C. REVISED DESIGN GOALS

This limitation of approximately +/- 12 volts as a maximum input voltage resulted in a change in design parameters based on the a system rational similar to that presented in Chapter II, section A. In this case the maximum number of folds was 5.1 from Equation

13. A minimum modulus of 3 was chosen, along with other pair wise relatively prime moduli of 4 and 5. This decisions led to the selection of five bit resolution design with 31 output states. A derived voltage swing for this system was calculated to be +/- 11.22 volts. Figure 8 is shown with the oscilloscope cursors at the input voltage that would result in a peak to peak voltage of 22.4 volts across the minimum modulus.

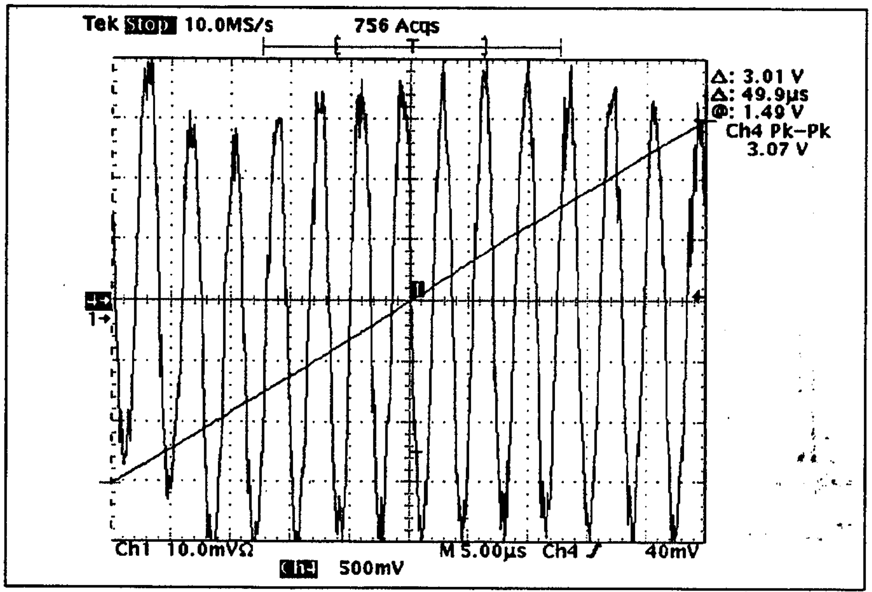


Figure 7. Example of Non-Uniform MZI Folding Pattern (+/- 30 V)

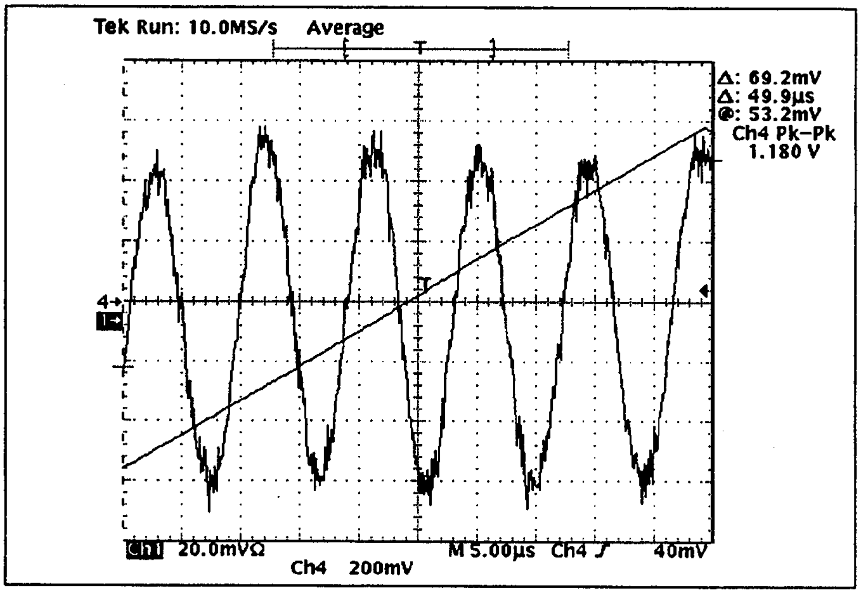


Figure 8. Example of Accepted MZI Folding Pattern (+/- 22.4V)

V. SYSTEM DESCRIPTION

A. ELECTRICAL

The electrical stages of the previous electrooptic analog to digital converter designs involved a binary decision process per moduli with subsequent encoding via "look up table" implementations. In the proposed design the system can be described around three basic stages; a comparator bank, priority encoder stage and output word encoder, see Figure 9. The unique basis for this project design was in the combination of three comparator bank outputs (raw or priority encoded) into a final output word. As stated in Chapter II, this was to be accomplished as combinational logic to avoid additional sample and hold time delays.

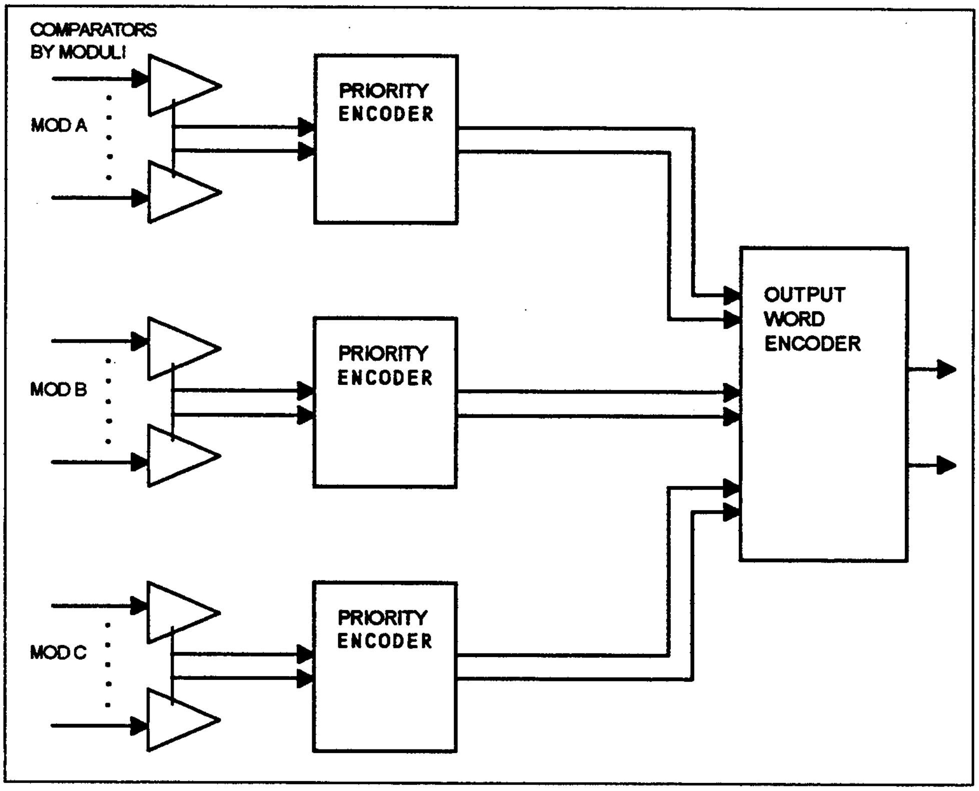


Figure 9. System Block Diagram

1. Prototype Overview

Three prototypes were built in support of this effort. The initial unit was based on LM-311 comparators and used Electrically Programmable Read Only Memory (EPROM) to implement the encoding of the logic stages to an output word. Interferometers were not available at this time therefore, a simulated input was used based on LabView software as described by Crowe (1995). The prototype allowed for a demonstration of the encoding logic and the effects of decimation window width versus output error states. The LM-311 was judged to be too slow for real time interferometer encoding applications and did not support Transistor-Transistor Logic (TTL) output without external circuitry.

The second generation prototype was envisioned to support an eight bit design but this design was curtailed after evaluation of non-uniform extinction ratios as discussed in Chapter II. Prior to this decision a full scale circuit development was completed. This included the choice of a new high speed TTL comparator (Analog Devices AD9698) and software development for programmable logic devices. This generation of encoding stage relied upon 22V10 logic functions to implement the priority encoder stages and EPROM devices for output word encoding.

The final design instrumented a resolution of five bits with a 40 nanosecond optical pulse width. By use of the AD9698 comparators, 22V10 devices and firmware development knowledge gained during the eight bit design, the development time for the 5 bit system was greatly reduced. Additional reductions in circuitry and simplifications were made due to the reduced number of output states.

2. Five Bit Circuit Description

Each moduli required a bank of comparators, always one comparator less than the respective modulus, functioning as a flash encoding stage. The latching function for the comparators was not used in this circuit thus allowing the output TTL level to follow the state of the comparator.

Threshold voltages for the comparators were created via a single potentiometer per comparator. This circuit functioned as a voltage divider across a single reference voltage for the system. A key aspect of this method of threshold generation was the ability to adjust the maximum input voltage (for the threshold levels) with one adjustment. This was in contrast to previous designs that used voltage divider networks of parallel fixed and variable resistors to establish each threshold. The single potentiometer per comparator threshold was simpler for this design due to the smaller number of thresholds per moduli. Comparator thresholds were calculated via MatLab code written by Yamakoshi, (1995). It is significant to note these levels were non-linear across the cosine squared intensity function therefore the traditional voltage threshold circuitry was not applicable for this case. Table 2 shows the threshold values used in this project.

A significant step was made in the encoding stages of the 5 bit design compared to higher resolution designs. In this case a single Lattice 22V10-15 Generic Array Logic (GAL) device was used to combine the priority encoder stages and EPROM output word encoder of the previous design. This was only possible due the reduced states of the 5 bit versus eight bit design (i.e. 31 states compared to 256) however the results show this to be a significant step in expected conversion time. These devices were rated at a propagation delay of 15 nanosecond vice the projected delay of 135 nanosecond for a combination GAL and EPROM design.

Comparator #	Normalized Threshold	Actual Threshold
	Modulus 3 and Error Detection (15% decimation)	
1	0.0015	0.0049
2	0.2168	0.6938
3	0.2847	0.9112
4	0.7153	2.2888
5	0.7832	2.5062
6	0.9985	3.1951
	Modulus 4	
1	0.1464	0.4686
2	0.5	1.6
3	0.8535	2.7313
	Modulus 5	
1	0.0955	0.3056
2	0.3455	1.1055
3	0.6545	2.0944
4	0.9045	2.8944

Table 2. Comparator Threshold Values

One feature of the compilers that complemented the low number of states condition was the ability to enter the desired logic via a truth table format. A sample of such a series of entries is shown below as Table 3. Note i1 and i2 are comparator outputs for modulus 3 comparator 1 and 2 respectively, hence i3, i4 and i5 are modulus 4 comparator 1 through 3 and i6 through i9 are modulus 5 comparator 1 through 4. As shown the initial state input would be 000000000 with a progression that corresponds to the thermometer code output of the comparator banks.

i9i8i7i6i5i4i3i2i1i0	o5o4o3o2o1o0
0 0 0 0 0 0 0 0 0	0 0 0 0 0
0 0 0 1 0 0 1 0 1	0 0 0 0 1
0 0 1 1 0 1 1 1 1	0 0 0 1 1
....	....
0 0 0 0 0 0 1 0 0	1 1 1 1 0
0 0 0 1 0 0 0 0 1	1 1 1 1 1

Table 3. Example of Encoder Firmware

For higher bit resolution systems this single chip encoding scheme would probably be implemented as multiple stages of logic as shown in Figure 9. The comparator bank output encoding would then be divided into a priority encoder and an output word encoder. This division by function is due to product term limitations on the programmable logic devices. However, the single encoder method may have application for the higher resolution designs if appropriate optimization software and Very Large Scale Integration (VLSI) devices are used.

The code for these devices was compiled via the Texas Instruments Prologic software system. This system has a basic minimization routine but lacks a "packaging" function to optimize the code to the device used. This function was performed manually in this case by matching the product terms created by the minimization routine and the available capabilities of the 22V10. Programming details for various logic devices used in the course of this research are provided in Appendix A for reference.

Error checking was implemented from the outputs of the comparator bank of the lowest moduli. As described in Chapter III, section C, it was necessary to use $2(m_i\text{-}1) + 2$ comparators to provided for detection of ambiguous states. This comparator bank served a dual purpose as output to the word encoder for moduli 3 and error checking. The lower output of each window detector was used for the moduli 3 input to the word encoder. This was effective since any state within this band would be detected as an error and eliminated by the error correction circuit, therefore an actual comparator dedicated to modulus 3 thresholds was not required.

B. OPTICAL

The optical bench accepted for use was designed by Crowe (1995) and is shown as Figure 6. In this design the laser pulse is generated via a function generator saw tooth waveform triggering the digital input of the BCP-410 laser transmitter. The laser pulse is then passed through a four way splitter, various couplers and then input to the MZI for phase modulation. The electrical signal used to phase modulate the signal is shown as a generic radio frequency input passed through a four way power splitter, variable attenuators, a "bias T" mixing element for application of a DC voltage offset and then applied to the electrode inputs of the MZI. The resultant phase modulated optical pulse is detected and amplified prior to the comparator input stage of the electrical encoding circuitry.

1. Deficiencies and Modifications

A number of deficiencies in this design were noted during the initial testing phase with the electrical stages. Proposed solutions to these deficiencies are presented in the following sections and are summarized in Figure 10. As this design matures it is anticipated that other modifications will be necessary to accommodate criteria such as other interferometer configurations or increasing bandwidth requirements. The proposed solutions represent a static test configuration for this development stage.

a. Attenuation

The original optical bench design used passive resistance networks after a common gain stage to achieve the attenuation factors necessary for modification of a modulus to a desired folding period. These devices were found to be unacceptable due to limitations on the input voltage range and loading effects upon the gain stage. A solution was required that would allow amplification of a reference input (typically from a function generator 50Ω output for testing) with individual control of the gain of each channel to achieve the desired attenuation factor. As shown in Figure 10, a Tektronics AM-501 laboratory standard operational amplifier stage was chosen to provide variable gain with a large voltage range.

The AM-501 op-amps provide for an unusually large voltage swing across the output (+/- 40V), and dependent upon the configuration, can allow for variable gain. This variable gain characteristic was used to provide for an attenuation effect, when compared to the reference voltage of the minimum modulus, while also providing for a sufficient voltage across the interferometer to generate enough folds. Details of this circuit are shown as Figure 11. In this diagram the potentiometers in combination with the feedback resistors in the inverting path allow for gain adjustment to provide the required attenuation effect between the moduli. The highest gain factor is for the minimum modulus and in this case was 13 dB. The bandwidth for this stage was approximately 500 kHz. No adverse loading effects were noted from the interferometers.

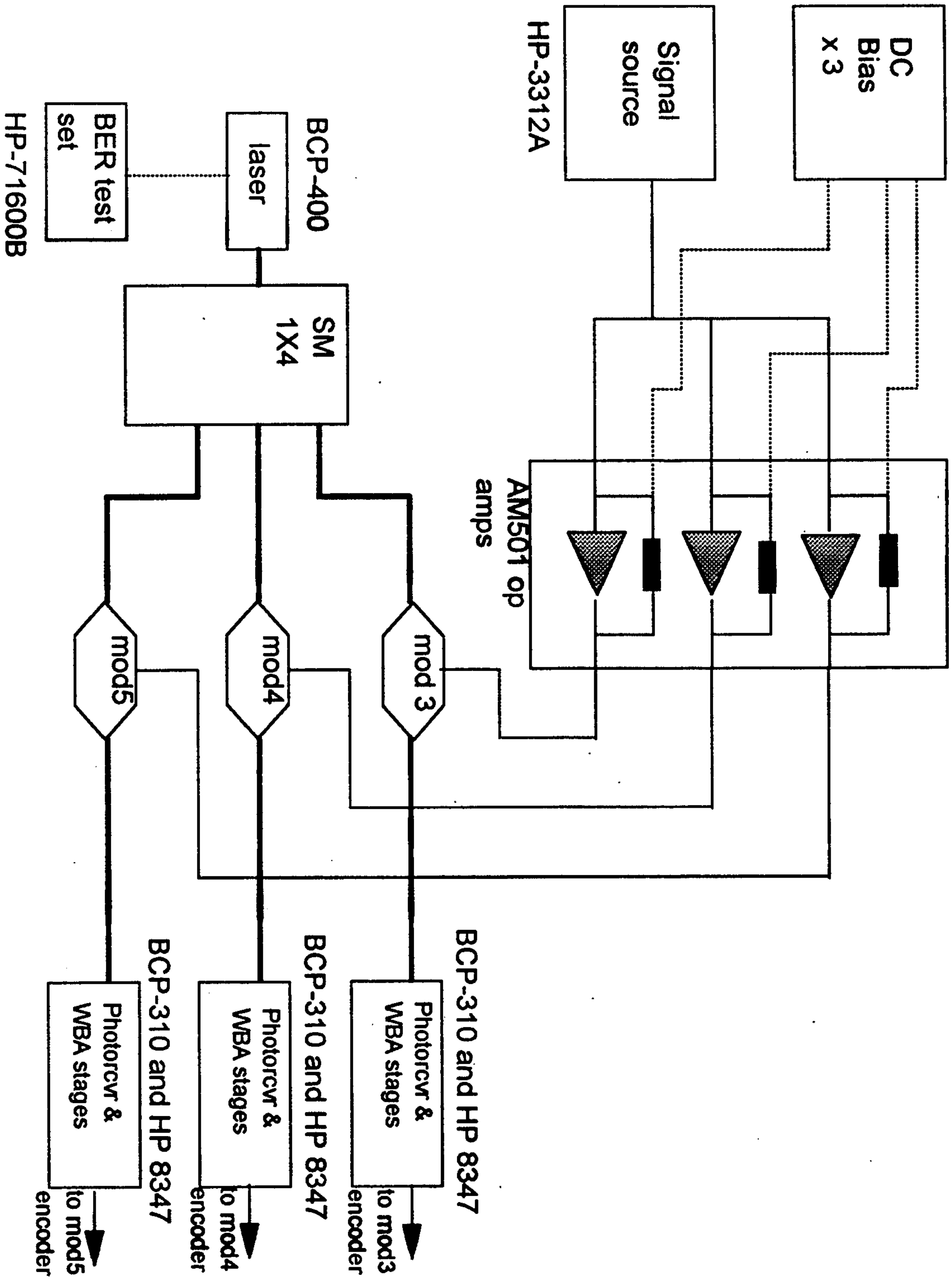


Figure 10. Revised Optical Bench

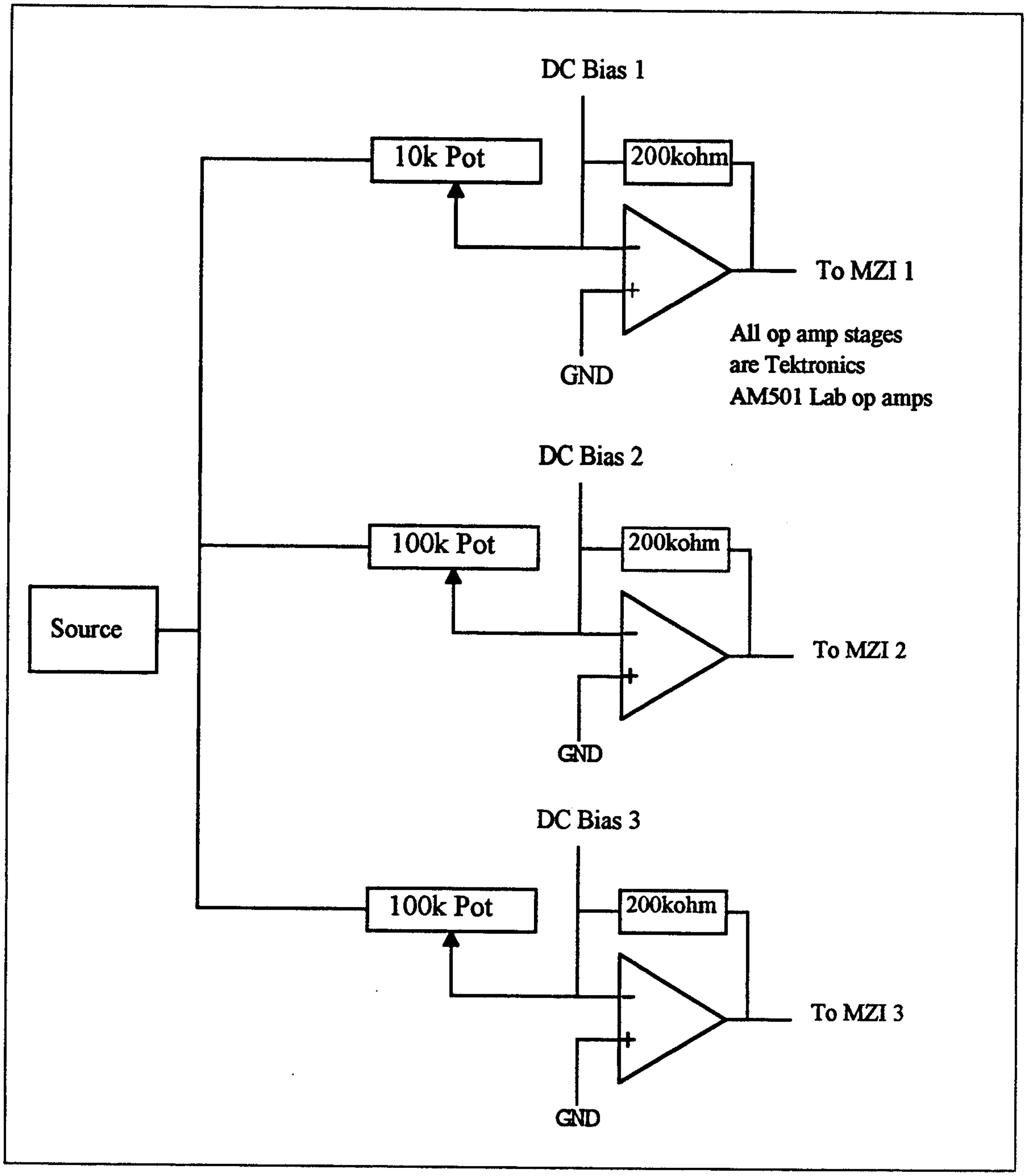


Figure 11. Attenuation Scheme for Five Bit Design

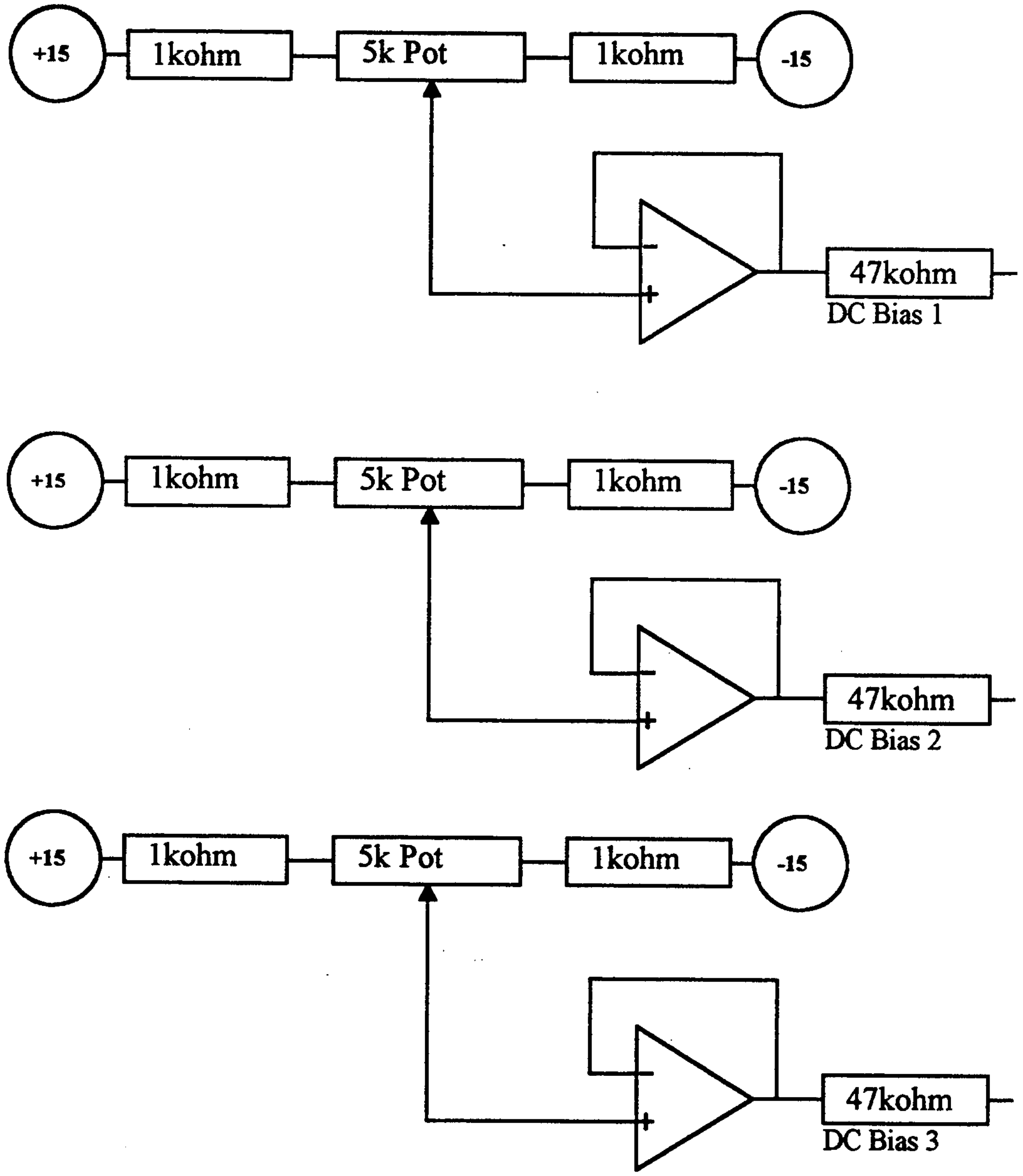
b. Interferometer DC Bias

The function of applying a DC bias to the MZI system was to establish a common reference point or initial state for the phase modulated waveforms. This reference to a initial state was necessary due to the fact that all three of the MZIs used were of similar design and construction (one of the cost benefits of this design) but they were electrically altered by an attenuation factor as a means of generating the desired folding period, see Equation 8. A small shift in the DC operating point compensated for this effect and resulted in a common negative referenced initial state for the system.

The original bench configuration used a "bias T" mixer function to provide this capability. However it was found that this device distorted low frequency waveforms and was unacceptable for dynamic system testing. The previous modification for attenuation adjustment provided the opportunity to apply the DC bias as a summing function to the operational amplifier inputs. A circuit to provide this bias is shown as Figure 12. The circuit selected was a simple voltage divider configuration with a voltage follower used to provide for impedance matching. This circuit was chosen for simplicity, small number of components required (the LM-324 is a quad package), and isolation.

c. Signal Path Length Differences

The final modification to the optical bench was made due to signal path length differences. The primary cause of the relative time differences was found to be variations in the length of optical fiber cabling attached to the interferometer. This length included the fiber fused to each interferometer plus any associated patch cords in the optical path from the single mode 1X4 splitter up to the BCP-310 optical receiver. Electrical path length differences were also considered in this signal path. A representative example of the timing differences is shown in Figure 13.



All op amps shown are part of an LM324 (quad op amp package), Vcc=+/- 15VDC
All Vref are +/- 15 VDC

Figure 12. DC Bias for Initial State Adjustment

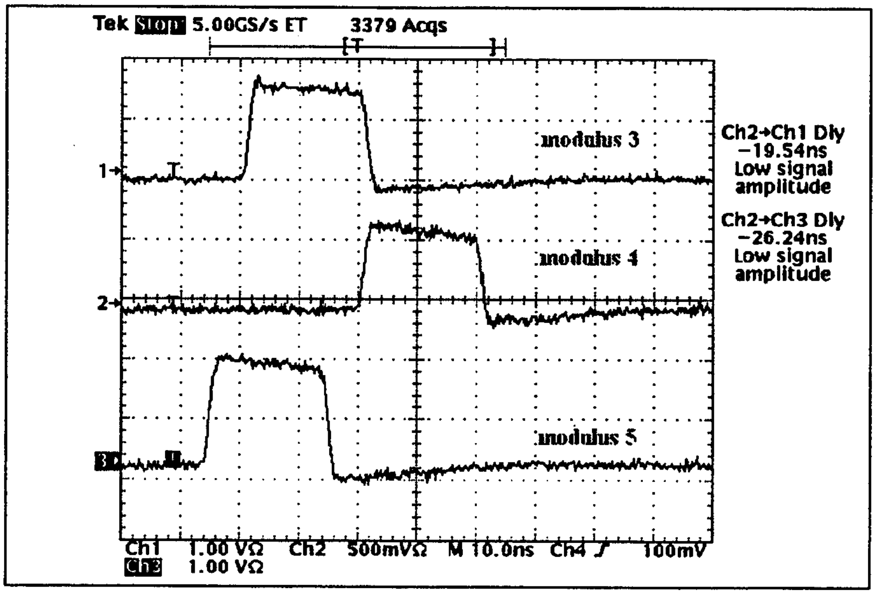


Figure 13. Typical Initial Signal Path Timing

To compensate for these delays in the optical path it was decided to use the pulse path with the largest initial delay as a reference and via a length of optical fiber generate a corresponding delay (per moduli) to align the pulses within a reasonable tolerance. To calculate this delay for a given length of fiber, the velocity of propagation through the optical fiber was required. The relationship chosen was based on the optical fiber index of refraction (*n*), velocity of propagation (*V*), and the speed of light (*c*)

$$n = \frac{c}{V} \tag{17}$$

and solving for V. The index of refraction for some of the fiber paths was not known but estimates were available from industry standards, this value was estimated to be approximately 1.4776. This resulted in a calculated value of 0.203 m/nsec delay.

Based on the preceeding calculations two delay line patch cords were made and installed in the optical path. The results of this correction are shown in Figure 14. As shown and subsequently measured by digital storage oscilloscope a worst case time

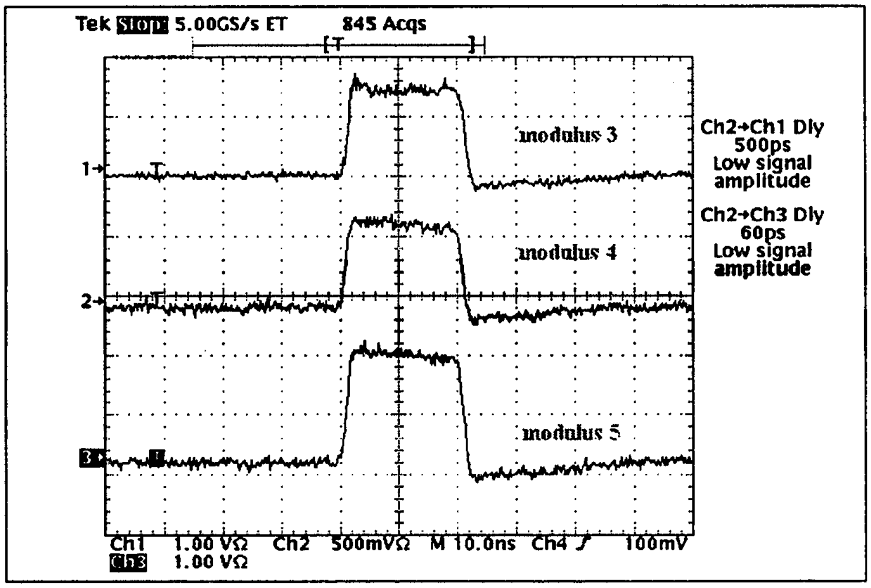


Figure 14. Time Aligned Signal Path

difference of 500 picosecond was achieved. This value was accepted as within the tolerance of the electrical path used and suitable for this prototype.

d. Laser Pulse Generation

The system as described by Crowe (1995) used a sawtooth waveform crossing Emitter Coupled Logic (ECL) thresholds on the laser transmitter for optical pulse generation. This method provides for a infinitely variable pulse width within the capabilities of the applicable transmitter but lacks a easily definable pulse jitter time. This variable has been widely accepted as one of the key elements in waveform sampling systems and therefore another standard for optical pulse generation was used.

The lowest pulse jitter source available to the Optical Laboratory at the time of testing was found on a Hewlett-Packard model 71600B Bit Error Rate Test Set. This unit has a specified 10 picosececond rms pulse jitter, with wide range of clock frequencies and user defined word length and pattern. This variable word length and pattern was used in conjunction with the clock rate to generate highly stable pulse widths and repetition rates. As an example, for a 40 nanosecond pulse width and a pulse repetition interval of 200 nanoseconds a twenty bit word was used at 100 MHz with 4 bits set to "one." This procedure is documented in Appendix B, section A.1.

2. Calibration Overview

In conventional analog to digital converters minimal consideration is required for calibration of the system due to the nature of the sampling systems and maturity of the technology. These samplers are sufficiently modeled as a switch/capacitor systems with well defined input parameters. This is not the case for developmental prototype systems such as the MZI based analog to digital converter.

Specifically, the three areas discussed in the previous section require alignment for proper operation of the modulator subsection. Since these procedures will vary with the equipment used, a generic discussion is presented with specifics of this system deferred to Appendix B for detailed procedures. In general, the attenuation and DC bias adjustments are performed while the laser is in a continuous wave rather than pulsed mode and the electrical source for these tests should be a ramped voltage from the maximum negative to maximum positive input voltage. Note that this is not the breakdown voltage or V_{max} of the interferometer but the maximum intended input voltage. A digital storage oscilloscope (four channel) has been found to be the most useful tool for this purpose.

a. Attenuation

Attenuation was achieved in this system as described in Chapter V, section A.1., via adjustment of an input gain circuit. The function of this attenuation is to create a folded modulus referenced to the lowest moduli of the system. This was achieved by first measuring the folding period of a segment of the lowest moduli to be used as a reference. The desired folding period for the other moduli could then be calculated by multiplying the reference period by a factor of the desired moduli divided by the reference moduli. As an example, suppose the folding period of the reference modulus (modulus 3, for example) as shown in Figure 15 was 10 microsecond (using the center graticule as the reference, trace 1 is modulus 3, etc) and the desired modulus was 4. The desired period for modulus 4 would be 10 microseconds multiplied by 4/3 or 13.33 microseconds. The gain of this stage (modulus 4) was then adjusted for this folding period and equivalently for the remaining modulus.

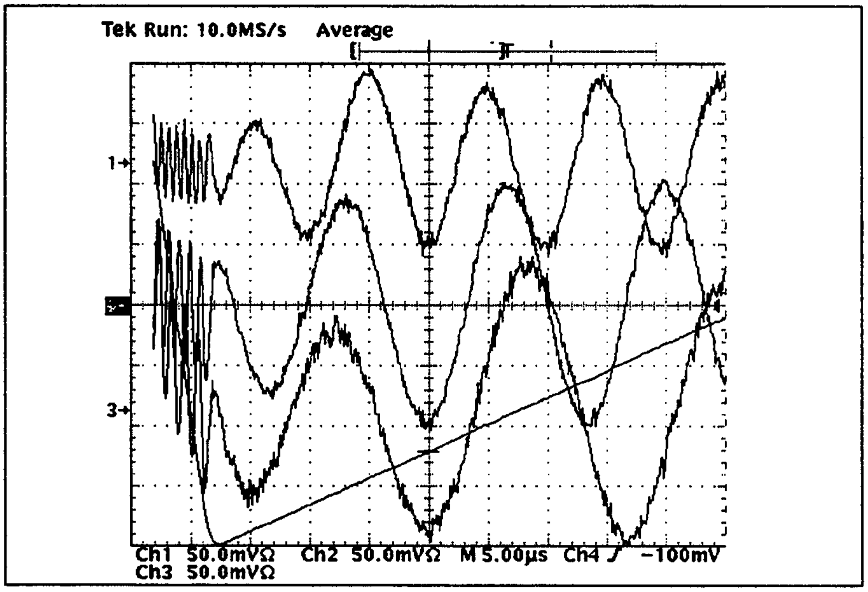


Figure 15. Attenuation Adjustment Example

b. DC Bias Adjustment

The function of DC bias in this system is to allow for shifting of the MZI operating points to allow for a voltage synchronized starting point for all moduli. This was required due to the modification of the folding period by attenuation and minor variations in the MZI operating points. As shown in Figure 16 and as would be expected of differing moduli, there is no easily predictable initial state point to establish. The method chosen was to overlay the input ramp and find the negative voltage point (input voltage shown on the figures) of the dynamic range. This should be the one point where the waveforms were in phase, the ultimate goal of the DC bias application is to align this instance of synchronization across each modulus used and use this point as the lowest state for encoding the output word.

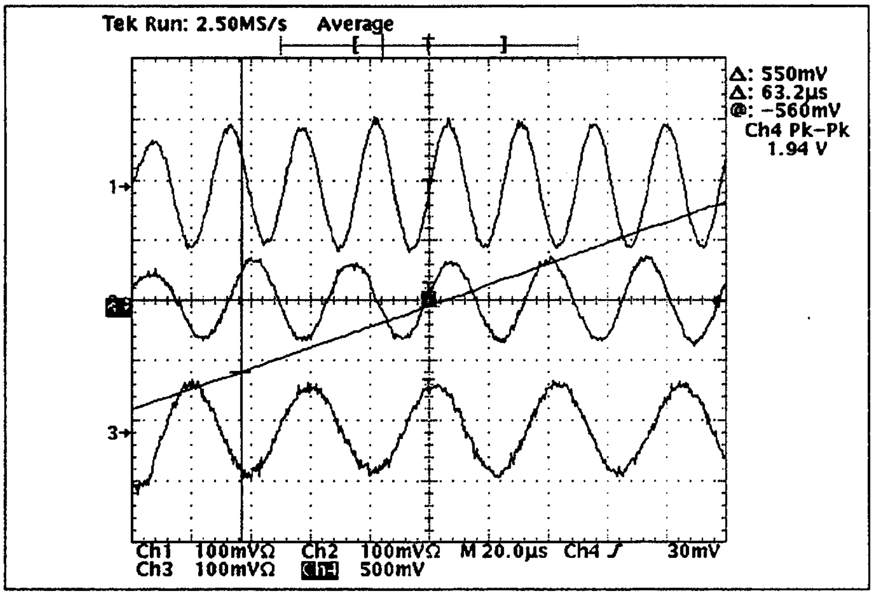


Figure 16. Folded Waveform Prior to Alignment

The most efficient method found for this alignment was to extend the operating region of the MZI system beyond the desired maximum input range a small number of folds then align the existing folds at the desired maximum negative value. A typical alignment is shown as Figure 17. Note the cursor position on the left side of the display. A fine adjustment of this value can also be performed after the initial adjustment by using the system in the pulsed mode. Using a DC source to present the most negative input voltage to the electrical system and monitoring the pulsed output of the interferometers will allow for an adjustment of the DC bias to achieve a minimum intensity level.

c. Time Alignment

The signal path discussion and optical delay line adjustments of Chapter V, section B.1.c., is of sufficient detail for this alignment step. However, care must be taken to ensure that the complete signal path is evaluated for time alignment. This should include all input signal cabling, wideband amplifier, and circuit card assemble connections.

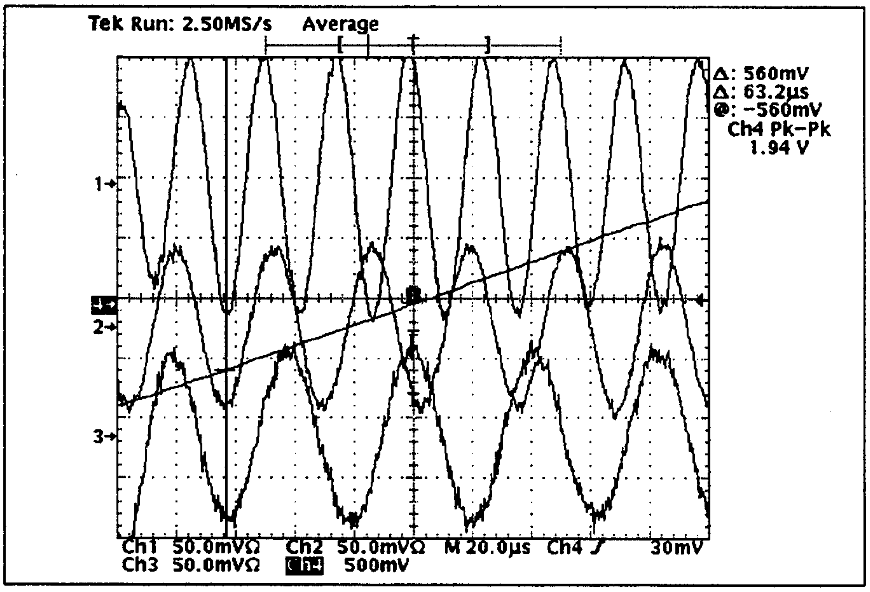


Figure 17. Folded Waveform After Alignment

d. Photodetector Gain

The final adjustment required in the analog signal path was the BCP-310 photodetector gain. This allowed for variations in maximum pulse height due to factors such as optical path loss differences or amplitude changes from pulse width changes in testing. It should be noted as well that this was the only point to vary the gain of the analog signal after conversion from optical to electrical (i.e. all subsequent gain stages were fixed magnitude).

The procedure was based on application of a DC level to the analog signal input path to the MZI and adjustment of this value to achieve a maximum pulse height (adjusting each modulus independently) measured at the respective modulus comparator circuit input. The TTL output of the comparator bank was monitored while the gain was adjusted until all comparators within the bank were firing but not over driven. This method allowed for maximum operating range regardless of the applied reference voltage.

VI. TEST RESULTS

A. TEST CONFIGURATION

The following sections discuss the testing phase for the five bit electrooptic analog to digital converter. The testing consisted of static electrical testing for verification of the operation of the encoding circuit and dynamic testing for derivation of a DC transfer function. Test assumptions and minor modifications made to the system to facilitate testing are discussed in the relevant sections. The system was configured as shown in Figure 18. (All figures for this chapter are at the end.)

B. STATIC TESTING

1. Pulse Response

The pulse response test was used as a first step for circuit card verification after construction. The test was envisioned to provide a method of testing that was not interferometer based and easily modified for troubleshooting purposes. In this test a pulse generator is used to simulate the interferometer output when pulsed via the laser. The pulse is routed to an encoder bank with the outputs of the comparators monitored via the Hewlett-Packard 16500B logic analyzer.

A typical application of this test is shown in Figure 19. In this case the pulse generator output was connected to the modulus 3 comparator bank and adjusted for a 10 MHz pulse mode (100 nanosecond pulse, 50% duty cycle), variable height for diagnostic purposes. Note the use of $2(m_i\text{-}1)+2$ comparators in this stage for implementation of the error detecting circuitry as discussed in Chapter III, section C. In this case the comparator states, as shown on the logic analyzer vertical legend, were PAR1 though PAR 6 (low to high threshold) for modulus 3 and the error windows. As seen in Figure 19, all of the comparators in this bank responded properly to the full range sample pulse. In addition, examination of Figure 19 shows a more narrow pulse width for the logic lines of CMP3_2 through PAR 6. An analysis of the pulse generator output found significant rise time limitations at this frequency (e.g. rounding of the pulse) and confirmed the proper operation of the comparators.

2. Output Word Encoding Tests

For this demonstration the optical system was connected to the comparator bank and the interferometers were optically pulsed with a variable DC level applied. This produced a very fast rise time pulse output of variable amplitude that was more representative of the intended application than the previous pulse generator output.

The purpose of this test was to exercise the encoding system with a constant or slowly varying input environment. Figure 20 shows the results of a typical encoded word versus comparator states. The additional legends on the logic analyzer represent the comparator states CMP4_1 through CMP4_3 for modulus 4, and CMP5_1 through CMP5_4 for modulus 5. The encoded output word is represented by OUT1LS through OUT5MS for least to most significant bit respectively. Note on the figure that the states to encode for this example were modulus 3 comparator 1, modulus 4 comparator 1 and 2, and no comparators on modulus 5 which encoded to an output word of 01010 as designed by the firmware. Programming for this firmware is covered in Appendix A.

A typical range for testing covered zero to the voltage reference used on the comparator thresholds, for this case 0 to 3.2 volts. Use of this range exercised a convenient series of states representing the first fold of the system. Other states were more difficult to enable from the comparator banks but were tested via manual application of logic levels to the output word encoding integrated circuit.

3. Error Detection Tests

Testing for error detection involved comparison of the logic states from the modulus 3 comparator bank to the logical output of the parity encoder chip. Figure 21 depicts such a test. Note the even and odd outputs of the parity encoder chip are available for use and are labeled as PO0 and PO1 respectively. For this test an external signal generator was used again at a 10 MHz pulse, 50% duty cycle. The figure illustrates a condition of three comparators of the error detection circuitry "firing" and the resulting odd parity condition. Also note for this encoder, zero states are considered even, hence the toggle to even between pulses.

C. DYNAMIC TESTING

1. Signal Integrity

Signal integrity is an essential component to the proper operation of a sampling system based on pulse height encoding. Variations in pulse width (jitter), height and the uniformity of the pulse height across the width of the pulse are the key characteristics for analysis. In this analysis pulse height variation was found to be a significant factor. A subjective comparison of pulse characteristics is shown in Figures 22, 23 and 24. For reference in these figures the volts/division is shown in the lower left corner, time/division is in the midsection of the display preceded by an "M", trigger source and level are in the lower right, and on Figures 23 and 24 the " Δ ... @" value in the upper right indicates the difference between and relative locations of the horizontal cursors placed across the variations cross the pulse width.

Figure 22 depicts the pulse generated for triggering the laser system followed by Figure 23 showing the pulse after detection, amplification and ideal termination into a 50 Ω load at the oscilloscope. The pulse as presented to the comparator bank is shown in Figure 24. This was captured via a X10 probe for minimal circuit interaction. Problems from the variations shown on Figure 24 are discussed in the respective sections.

2. Dynamic Signal Testing

This segment of the system testing applied low frequency waveforms to the system and evaluated the output of the analog to digital conversion process without error correcting. These signals were low frequency (1 kHz) sine and triangular waves. Input and output representative waveforms are shown as Figures 25 through 28.

The test system for this series of figures used the logic analyzer in the state analysis mode with an asynchronous 5 MHz clock to sample the output word states. The chart mode of the logic analyzer was used to convert the 5 bit output word into a decimal equivalent of the state. This state was then plotted versus sample number resulting in the equivalent of a digital to analog conversion of the samples.

An analysis of sampled waveforms shows a definite similarity between the input and output waveforms. The 32 state dynamic range of the system was exercised in these figures as shown by the range in the "Ymin" to "Ymax" windows of the logic analyzer (states 00 to 31). A subset of these values centered about the mid-range of states is obtained when the signal level is below the designed maximum levels.

This relatively low frequency analysis leads to a large oversampling of the input but does serve as a proof of concept for the use of multiple interferometer symmetrical number system based analog to digital converters. As anticipated there were error states that resulted from ambiguous encoding regions. These errors were also noted on the slow speed prototype design and anticipated (Pace, 1995). The asynchronous nature of the design also led to a large number of the states since the typical sample between optical pulses would be interpreted by the logic analyzer clocking system as a "zero" state vice the desired next sample.

3. Error Detection Performance

The function of the error detecting circuitry was to determine the validity of the samples based on the pulse voltage level within the lowest modulus and provide a logical accept/reject signal to a sample latch (based on the resulting parity). This latch would accept and pass the valid sample (odd parity) or reject the sample (even parity) and hold the last good sample (Yamakoshi, 1995). The key element of this process is in the determination of the pulse voltage within the thresholds set by the desired decimation bands. This proved to be a difficult task.

Figures 29 and 30 contrast the proper versus improper operation of the error detector. Figure 29 shows the lowest comparator in the modulus 3 ladder "firing" to indicate an acceptable region for encoding. These waveforms represent the correct operation of the circuit. In this case either parity line could be used in the design for application to the encoded word latch.

The converse is shown in Figure 30. In this case rapid fluctuations on the comparator outputs has toggled the parity encoder and results in an unusable output condition. The rapid fluctuations on the higher comparator levels are thought to be from variations of the pulse height across the pulse width. As shown the parity encoder tried to follow these variations and toggled the output states. Similar cases of encoder errors were also noticed when the comparators did not trigger at the same time along a rising pulse.

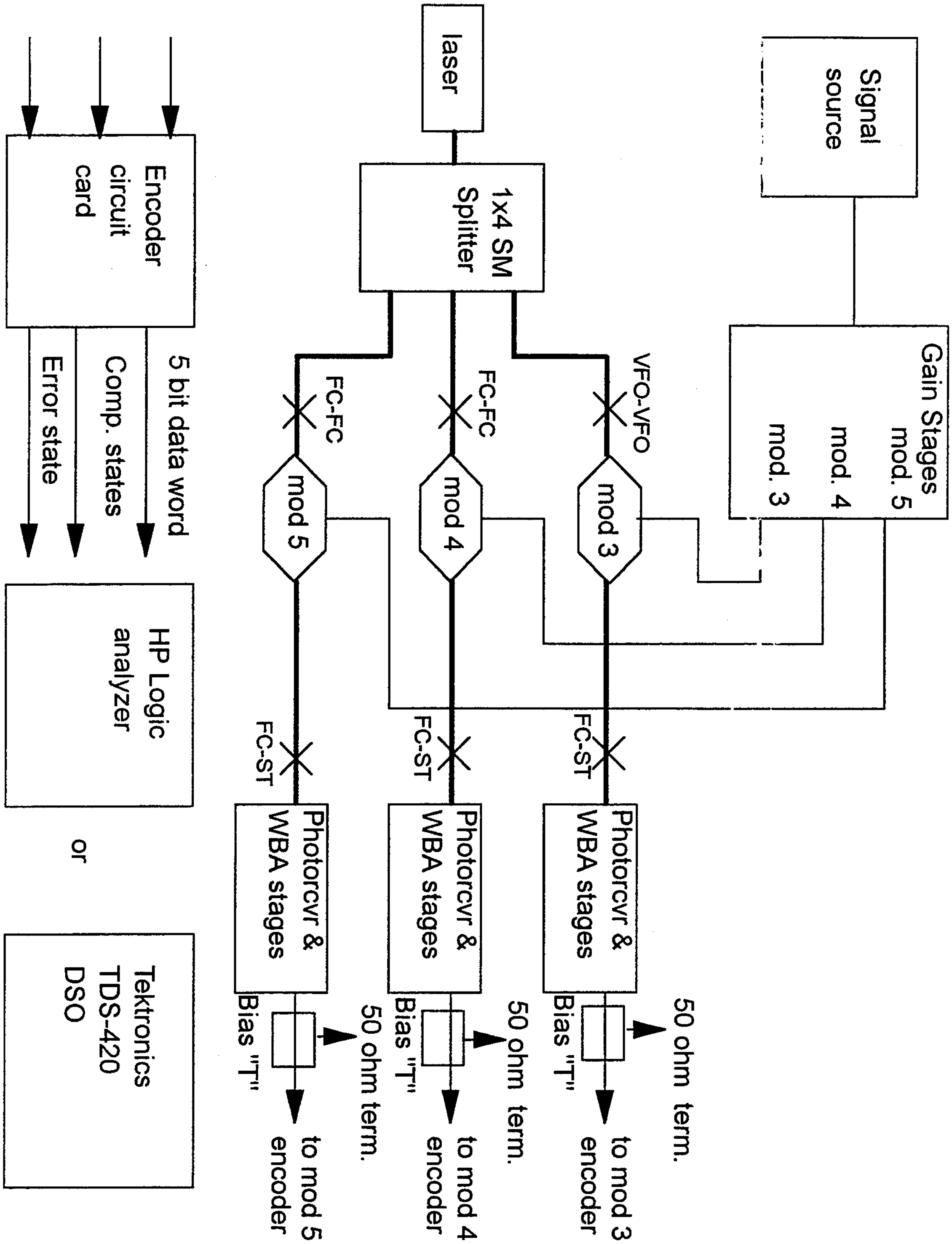
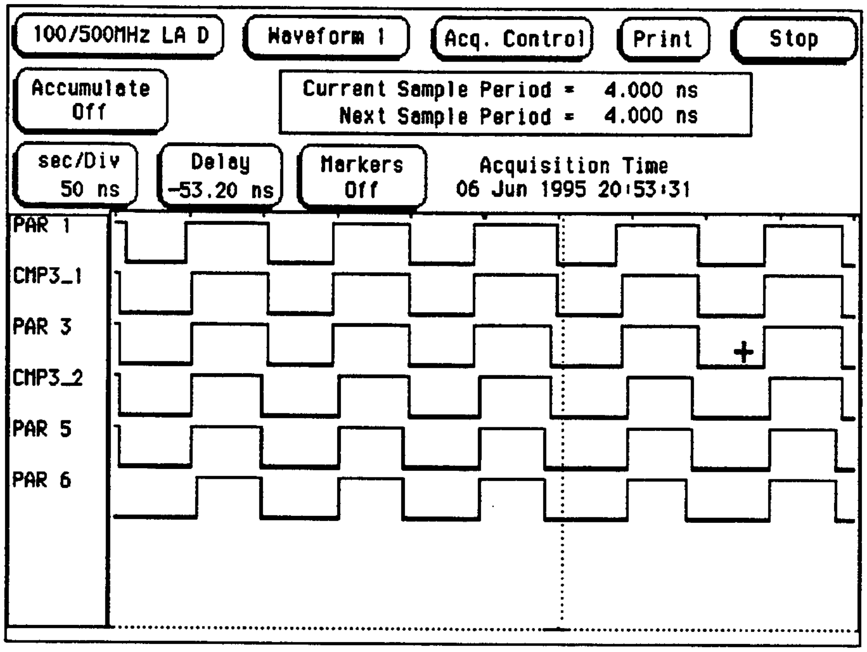


Figure 18. System Configuration for Testing



Accumulate Off

Current Sample Period = 4.000 ns

Next Sample Period = 4.000 ns

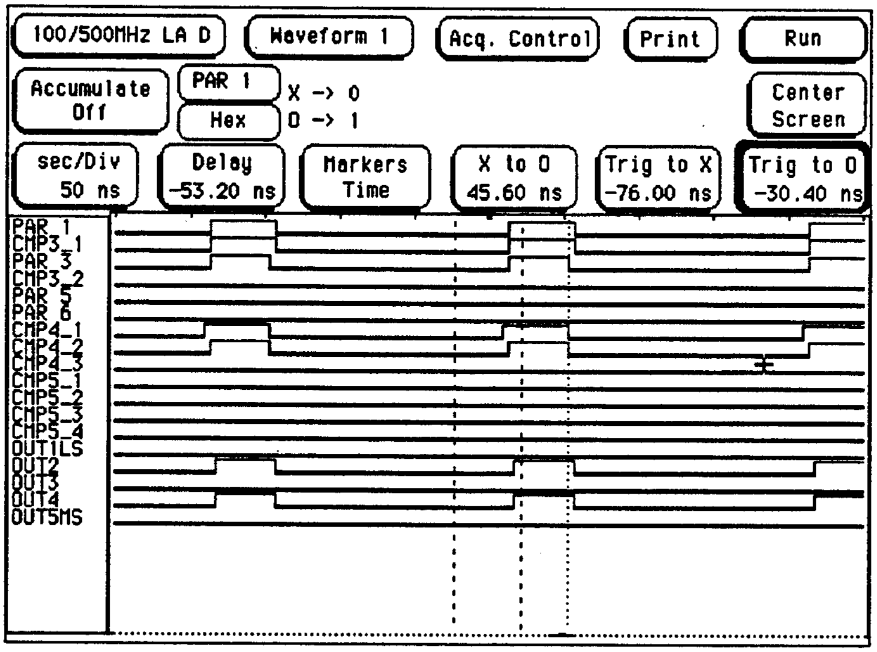
sec/Div 50 ns

Delay -53.20 ns

Markers Off

Acquisition Time 06 Jun 1995 20:53:31

Figure 19. Pulse Response Test



Accumulate Off

PAR 1 X -> 0

Hex 0 -> 1

sec/Div 50 ns

Delay -53.20 ns

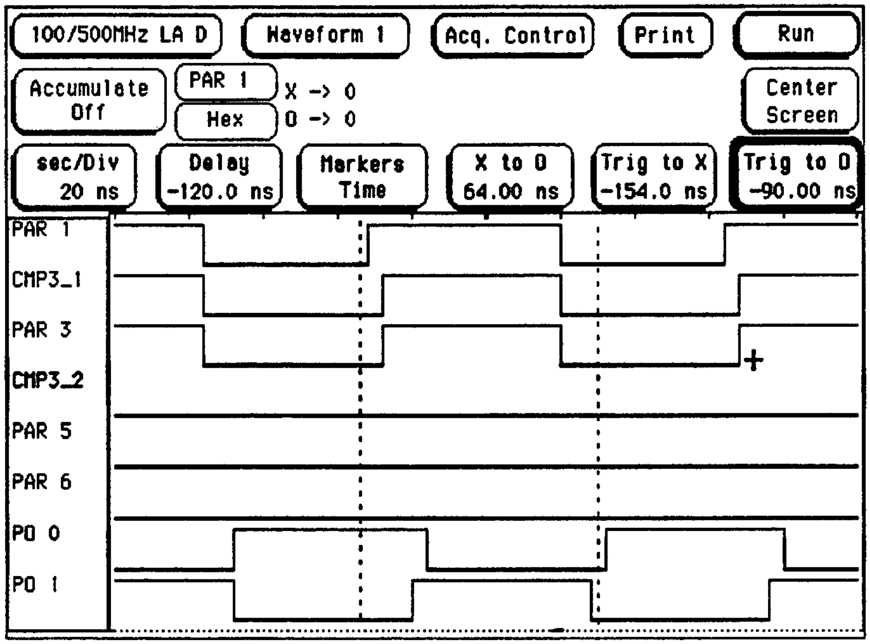
Markers Time

X to 0 45.60 ns

Trig to X -76.00 ns

Trig to 0 -30.40 ns

Figure 20. Output Word Encoding Test



Accumulate Off

PAR 1 X -> 0

Hex 0 -> 0

sec/Div 20 ns

Delay -120.0 ns

Markers Time

X to O 64.00 ns

Trig to X -154.0 ns

Trig to O -90.00 ns

Figure 21. Error Detection Test

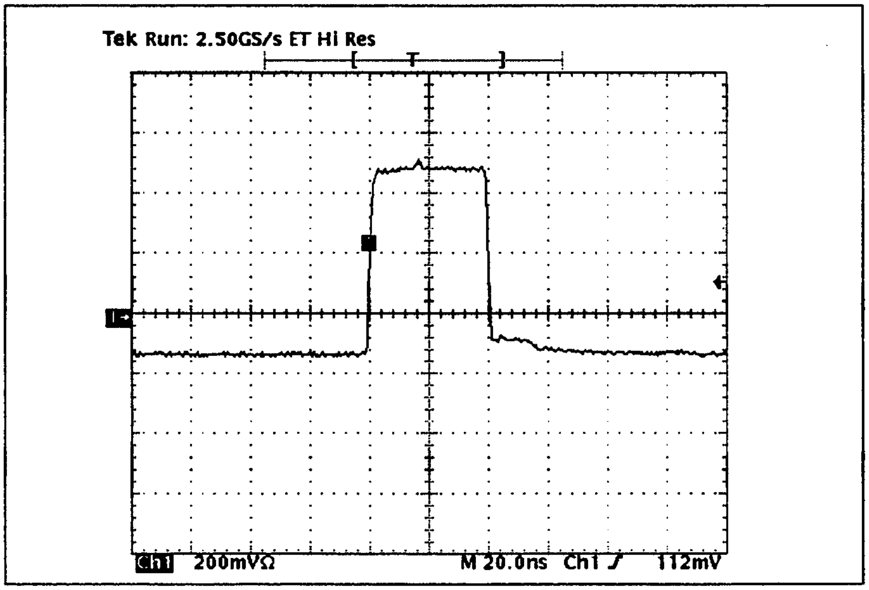


Figure 22. Laser Input Pulse

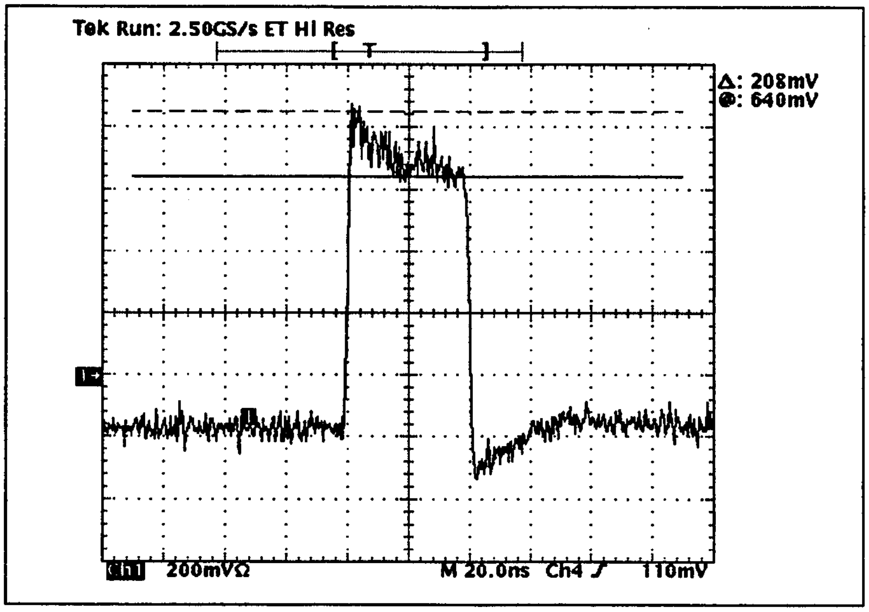


Figure 23. Pulse Response Test at Wide Band Amplifier Output

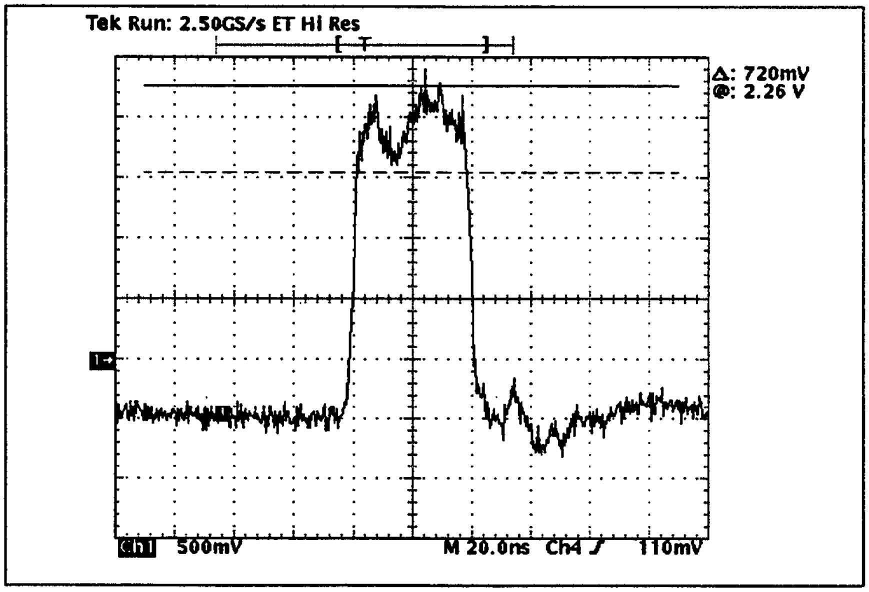


Figure 24. Pulse Response Test at Comparator Input

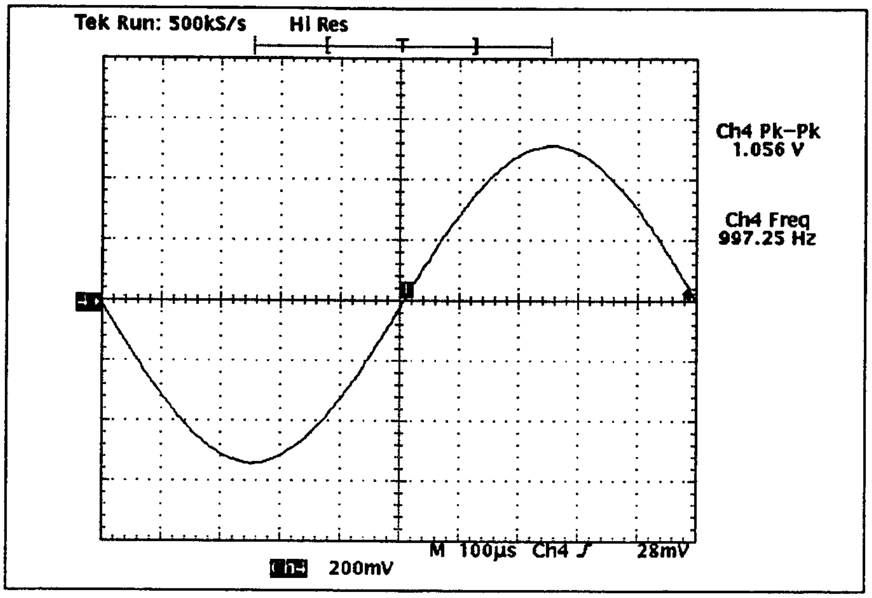
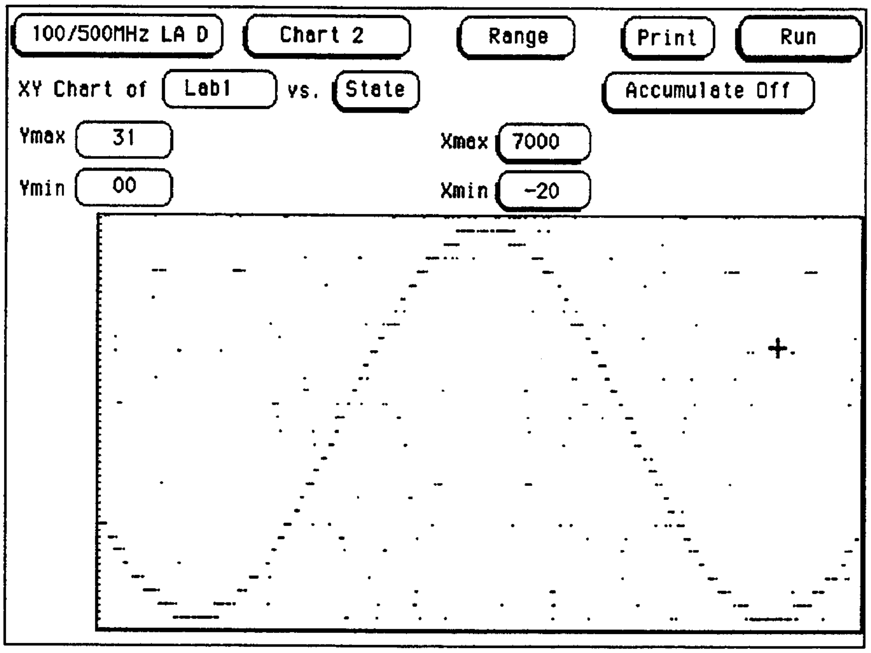


Figure 25. Sine Wave Input



XY Chart of Labl vs. State

Ymax 31

Ymin 00

Xmax 7000

Xmin -20

Figure 26. Logic Analyzer Chart Output for Sinusoidal Input

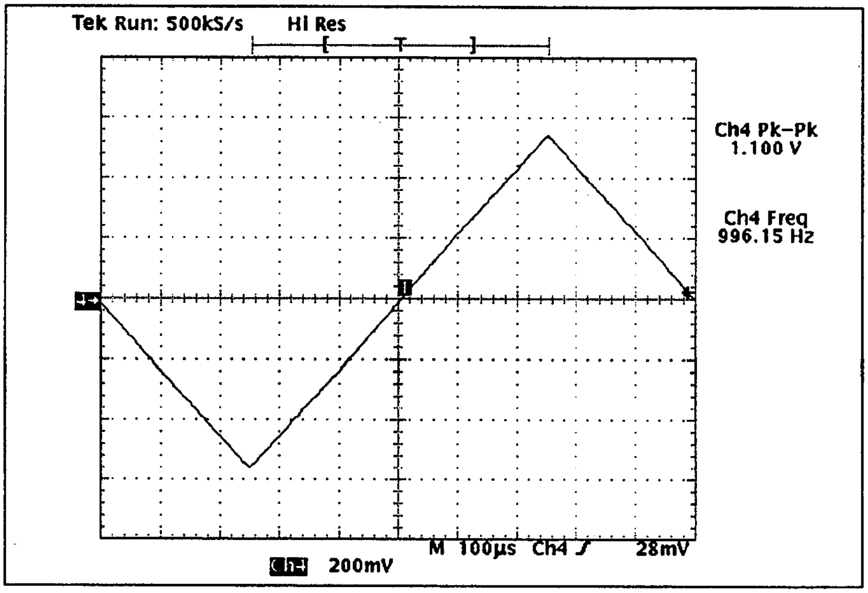
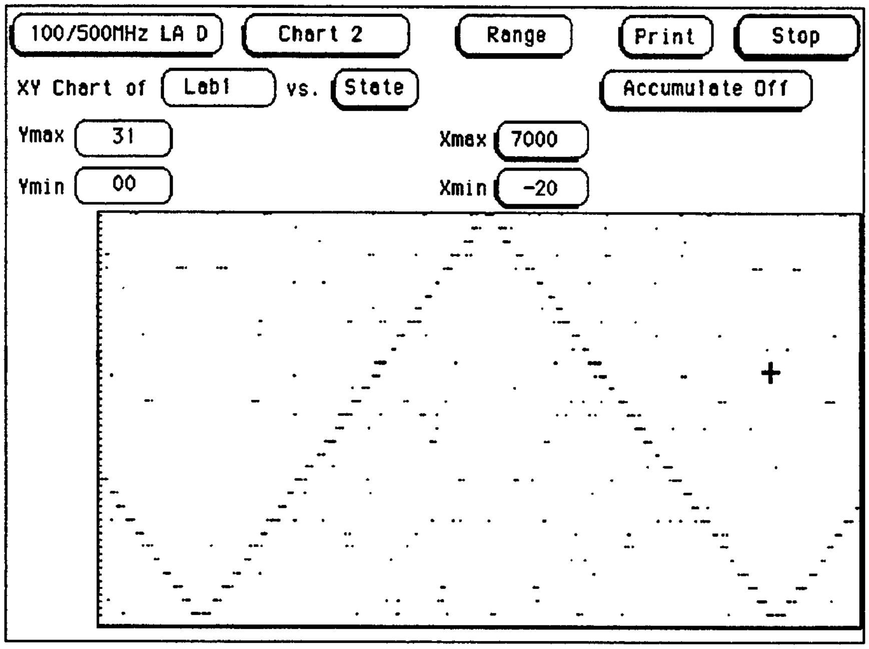


Figure 27. Triangular Wave Input



XY Chart of Labl vs. State

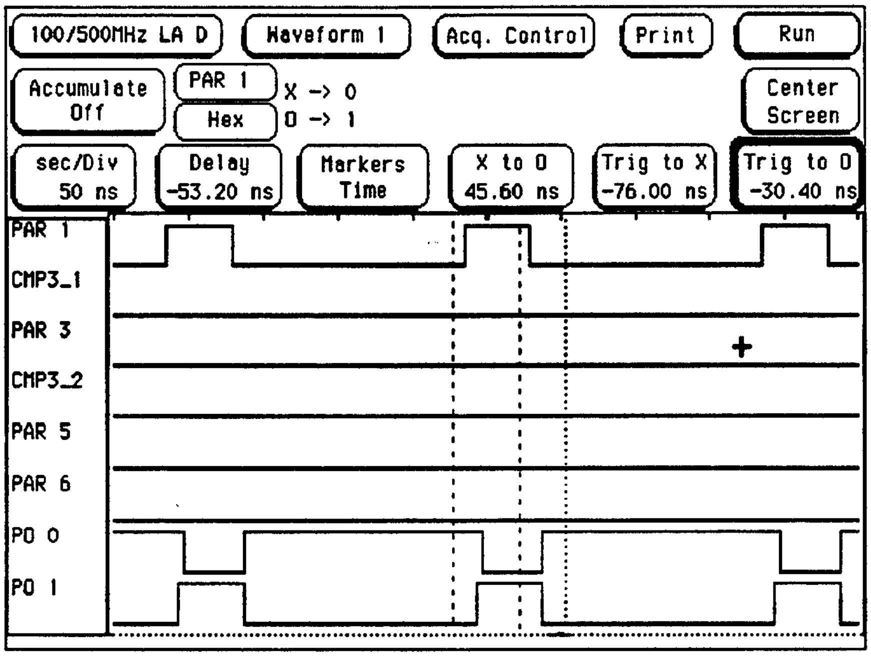
Ymax 31

Ymin 00

Xmax 7000

Xmin -20

Figure 28. Logic Analyzer Output for Triangular Input



Accumulate Off

PAR 1 X -> 0

Hex 0 -> 1

sec/Div 50 ns

Delay -53.20 ns

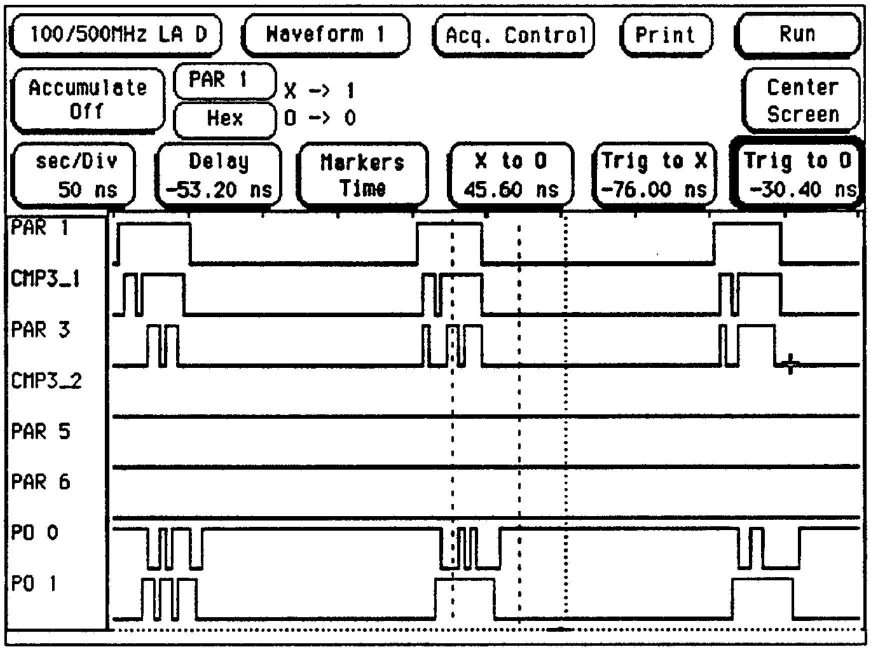
Markers Time

X to 0 45.60 ns

Trig to X -76.00 ns

Trig to 0 -30.40 ns

Figure 29. Error Detection Proper Performance



Accumulate Off

PAR 1 X -> 1

Hex 0 -> 0

sec/Div 50 ns

Delay -53.20 ns

Markers Time

X to 0 45.60 ns

Trig to X -76.00 ns

Trig to 0 -30.40 ns

Figure 30. Error Detection Improper Performance

VII. SUMMARY

Enhanced capability analog to digital converters are a key technology to the advancement of communication and signal processing. This thesis contributed to the advancement by constructing the first prototype sampling and symmetrical number system encoding scheme for a multiple interferometer based electrooptic analog to digital converter. As shown, the electrical processing concept for this system can be realized with commercially available components. However, for higher bit resolutions and smaller sampling pulse widths the requirements justify custom integrated circuits.

The goal of producing a five bit multiple interferometer system was partially completed but work still remains. The process requires refinement in the areas of signal integrity and error detection/correction. Mach-Zehnder interferometers designed specifically for this application are now in the laboratory for characterization. Higher power lasers are under consideration for increasing the optical power available to the photo-receivers. Use of these devices and the development of printed circuit card assemblies vice wire wrapped boards should provide for an enhancement of the system resolution to eight bits and higher. New techniques for electrically processing the interferometer outputs are also under development.

In summary, this thesis provides a proof of concept for dynamic use of the multiple interferometer based system and the utility of the symmetrical number system as an encoding scheme. Application of this technology in future systems could provide for the direct digitization of radio frequency bandwidth signals and the subsequent use of these signals in conventional digital distribution paths such as local area networks.

APPENDIX A. FIRMWARE

Programmable logic devices (PLD) were used wherever possible in this design. This allowed for testing of logic schemes not readily available from generic logic families. Two categories of devices were used: generic array logic (GAL) 22V10 devices and ultra-violet erasable electrically programmable read only memories (EPROM). Discussion of the firmware is divided by family with an overview of programming methods.

A. GAL FIRMWARE

Generic array logic devices were used extensively in the project due to flexibility and speed characteristics of the 22V10 logic family. A brief overview of device programming steps has been included for project continuity, see Figure 31.

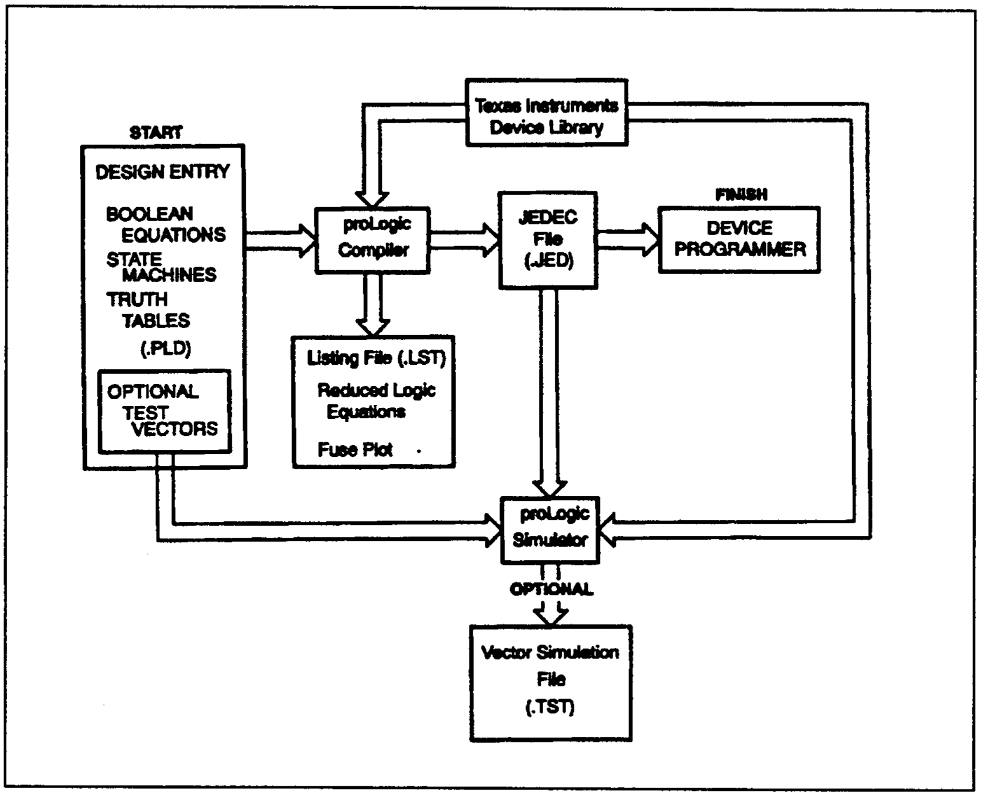


Figure 31. 22V10 Program Design Flowchart (From Texas Instruments, 1993)

The Texas Instruments Prologic compiler (V3.0) was used for all GAL development. No external "packaging" or extensive minimization (basic routines are included in the compiler) software were used, all decisions of this type were the result of manual comparisons of required product terms versus output logic macro cell capabilities.

1. Five Bit Encoder

This logic function evolved from the reduction in the dynamic range or number of states due to interferometer limitations. The firmware in this case consolidated the priority encoder and output word encoder into one 22V10 device. This not only reduced the component count from a minimum of four devices to one but also reduced the maximum conversion time from approximately 135 nanoseconds to 15 nanoseconds.

Conceptually the code evolved as a simple mapping from the symmetrical number system based output of the comparator banks to the output state. This effect can be seen by following one comparator bank output sequence through a few folds. As an example, i9 - i6 represent the output of modulus 5 highest comparator to lowest respectively. Following the source code the states progress as: 0000, 0001, 0011, 0111, 1111, 1111, 0111, 0011, 0001, 0000. When this sequence is combined with the outputs of the other moduli output states are formed. This combination was continued through the 31 states of the designed dynamic range thus forming a complete set. The source code for this device is attached at the end of this subsection with comments. Test vectors were omitted for brevity.

A feature of the 22V10 is the user selected option to operate the device in a combinational or registered mode. This application used the combinational mode but did not allocate the resources necessary for the registered mode in case future developmental work required the design to be clocked. For reference this change would require a minor software change and application of the desired clock to pin 1.

```
/* start of file */
title {function: sns decoder mod 3,4,5
      designer: Rick Walley,
           date: 13 Apr 95}
include p22v10;
define i1=pin2;  /*mod 3 comp 1 */
define i2=pin3;  /*mod 3 comp 2 */
define i3=pin4;  /*mod 4 comp 1 */
define i4=pin5;  /*mod 4 comp 2 */
define i5=pin6;  /*mod 4 comp 3 */
define i6=pin7;  /*mod 5 comp 1 */
define i7=pin8;  /*mod 5 comp 2 */
define i8=pin9;  /*mod 5 comp 3 */
define i9=pin10; /*mod 5 comp 4 */
 define o1=pin18; /* output lsb */
define o2=pin19;
define o3=pin20;
define o4=pin21;
define o5=pin17; /* output msb */
pin17.oe=1; /*output enable lines*/
pin18.oe=1;
pin19.oe=1;
pin20.oe=1;
pin21.oe=1;
truth_table{
i9 i8 i7 i6 i5 i4 i3 i2 i1 : o5 o4 o3 o2 o1;
 0 0 0 0 0 0 0 0 0 : 0 0 0 0 0;/*state 0*/
 0 0 0 1 0 0 1 0 1 : 0 0 0 0 1;/*state 1*/
 0 0 1 1 0 1 1 1 1 : 0 0 0 1 0;
 0 1 1 1 1 1 1 1 1 : 0 0 0 1 1;
 1 1 1 1 1 1 1 0 1 : 0 0 1 0 0;
 1 1 1 1 0 1 1 0 0 : 0 0 1 0 1;
 0 1 1 1 0 0 1 0 0 : 0 0 1 1 0;
 0 0 1 1 0 0 0 0 1 : 0 0 1 1 1;
 0 0 0 1 0 0 0 1 1 : 0 1 0 0 0;
 0 0 0 0 0 0 1 1 1 : 0 1 0 0 1;
 0 0 0 0 0 1 1 0 1 : 0 1 0 1 0;
 0 0 0 1 1 1 1 0 0 : 0 1 0 1 1;
 0 0 1 1 1 1 1 0 0 : 0 1 1 0 0;
 0 1 1 1 0 1 1 0 1 : 0 1 1 0 1;
 1 1 1 1 0 0 1 1 1 : 0 1 1 1 0;
 1 1 1 1 0 0 0 1 1 : 0 1 1 1 1;
 0 1 1 1 0 0 0 0 1 : 1 0 0 0 0;
0 0 1 1 0 0 1 0 0 : 1 0 0 0 1;
0 0 0 1 0 1 1 0 0 : 1 0 0 1 0;
0 0 0 0 1 1 1 0 1 : 1 0 0 1 1;
0 0 0 0 1 1 1 1 1 : 1 0 1 0 0;
0 0 0 1 0 1 1 1 1 : 1 0 1 0 1;
0 0 1 1 0 0 1 0 1 : 1 0 1 1 0;
0 1 1 1 0 0 0 0 0 : 1 0 1 1 1;
1 1 1 1 0 0 0 0 0 : 1 1 0 0 0;
1 1 1 1 0 0 1 0 1 : 1 1 0 0 1;
0 1 1 1 0 1 1 1 1 : 1 1 0 1 0;
0 0 1 1 1 1 1 1 1 : 1 1 0 1 1;
0 0 0 1 1 1 1 0 1 : 1 1 1 0 0;
0 0 0 0 0 1 1 0 0 : 1 1 1 0 1;
0 0 0 0 0 0 1 0 0 : 1 1 1 1 0;
0 0 0 1 0 0 0 0 1 : 1 1 1 1 1;/*state 31*/ }
```

2. PLD Based Priority Encoder

The priority encoding function was the key component in the generation of a "thermometer code" type of output from the comparator banks. In review, the priority encoder monitors a set of parallel inputs (from the comparator bank) and decodes a binary output based on the highest number of inputs presented. As an example, if 5 comparators were triggered then the priority encoder would present 0101 on the output.

A review of available devices versus PLD found a limitation in the number of inputs and cascading of the hardwired devices would have required development of a decoding scheme for the outputs. A programmable scheme was chosen that would allow the development of a generic device with up to 14 inputs therefore suitable to support up to a moduli 15 design. A complete source code listing for a 22V10 target device follows:

```
/*start of file*/
title{Function:  Priority encoder (14 bit),  rev 2
     Designer:  Rick Walley
       Date:    22 Aug 94}
include p22v10;
define i1 = pin2; /* lowest comparator input*/
define i2 = pin3;
define i3 = pin4;
define i4 = pin5;
define i5 = pin6;
define i6 = pin7;
define i7 = pin8;
define i8 = pin9;
define i9 = pin10;
define i10=  pin11;
define i11 = pin13;
define i12 = pin14;
define i13 = pin15;
define i14 = pin16; /*highest comparator input*/
define o1 = pin20; /*LSB out*/
define o2 = pin19;
define o3 = pin18;
define o4 = pin17;/*MSB out*/
pin20.oe = 1;/*output enable lines*/
pin19.oe = 1;
pin18.oe = 1;
pin17.oe = 1;
truth_table{
        i14 i13 i12 i11 i10 i9 i8 i7 i6 i5 i4 i3 i2 i1 : o4 o3 o2 o1;
/* 0 */  0  0  0  0  0  0 0 0 0 0 0 0 0 0 : 0 0 0 0 /* lowest state */
/* 1 */  0  0  0  0  0  0 0 0 0 0 0 0 0 1 : 0 0 0 1;
/* 2 */  0  0  0  0  0  0 0 0 0 0 0 0 1 1 : 0 0 1 0;
/* 3 */  0  0  0  0  0  0 0 0 0 0 0 1 1 1 : 0 0 1 1;
/* 4 */  0  0  0  0  0  0 0 0 0 0 1 1 1 1 : 0 1 0 0;
/* 5 */  0  0  0  0  0  0 0 0 0 1 1 1 1 1 : 0 1 0 1;
/* 6 */  0  0  0  0  0  0 0 0 1 1 1 1 1 1 : 0 1 1 0;
/* 7 */  0  0  0  0  0  0 0 1 1 1 1 1 1 1 : 0 1 1 1;
/* 8 */  0  0  0  0  0  0 1 1 1 1 1 1 1 1 : 1 0 0 0;
/* 9 */  0  0  0  0  0  1 1 1 1 1 1 1 1 1 : 1 0 0 1;
/*10 */  0  0  0  0  1  1 1 1 1 1 1 1 1 1 : 1 0 1 0;
/*11 */  0  0  0  1  1  1 1 1 1 1 1 1 1 1 : 1 0 1 1;
/*12 */  0  0  1  1  1  1 1 1 1 1 1 1 1 1 : 1 1 0 0;
/*13 */  0  1  1  1  1  1 1 1 1 1 1 1 1 1 : 1 1 0 1;
/*14 */  1  1  1  1  1  1 1 1 1 1 1 1 1 1 : 1 1 1 0; /highest state/
} /* end of file */
```

2. Priority encoder, second stage

For designs requiring a higher modulus than 15 (i.e., more than 14 comparators), a design was developed to multiplex the outputs of up to three of the generic priority encoding devices. This design has three groups of four bit data lines as inputs and presents a six bit word representing the overall priority encoder output. Source code follows:

```
/* start of file */
title{ Function: Priority encoder 2nd stage
     Designer: Rick Walley
          Date: 6 May 94}
include p22v10;
define i1 = pin1; /* low priority encoder lsb */
define i2 = pin2;
define i3 = pin3;
define i4 = pin4; /* low priority encoder msb */
define i5 = pin5; /*mid priority encoder lsb */
define i6 = pin6;
define i7 = pin7;
define i8 = pin8; /* mid priority encoder lsb */
define i9 = pin9; /* high priority encoder lsb */
define i10 = pin10;
define i11 = pin11;
define i12 = pin13; /* high priority encoder lsb */
define o1 = pin15; /* lsb out*/
define o2 = pin16;
define o3 = pin17;
define o4 = pin18;
define o5 = pin19;
define o6 = pin20; /* msb out*/
pin15.oe = 1; /* output enables */
pin16.oe = 1;
pin17.oe = 1;
pin18.oe = 1;
pin19.oe = 1;
pin20.oe = 1;
truth_table{
i12 i11 i10 i9 i8 i7 i6 i5 i4 i3 i2 i1 : o6 o5 o4 o3 o2 o1;
0  0  0  0 0 0 0 0 0 0 0 0 : 0 0 0 0 0 0; /* lowest state, 0*/
0  0  0  0 0 0 0 0 0 0 0 1  : 0 0 0 0 0 1;
0  0  0  0 0 0 0 0 0 0 1 0  : 0 0 0 0 1 0;
0  0  0  0 0 0 0 0 0 0 1 1  : 0 0 0 0 1 1;
0  0  0  0 0 0 0 0 0 1 0 0  : 0 0 0 1 0 0;
0  0  0  0 0 0 0 0 0 1 0 1  : 0 0 0 1 0 1;
0  0  0  0 0 0 0 0 0 1 1 0  : 0 0 0 1 1 0;
0  0  0  0 0 0 0 0 0 1 1 1  : 0 0 0 1 1 1;
0  0  0  0 0 0 0 0 1 0 0 0  : 0 0 1 0 0 0;
0  0  0  0 0 0 0 0 1 0 0 1  : 0 0 1 0 0 1;
0  0  0  0 0 0 0 0 1 0 1 0  : 0 0 1 0 1 0;
0  0  0  0 0 0 0 0 1 0 1 1  : 0 0 1 0 1 1;
0  0  0  0 0 0 0 0 1 1 0 0  : 0 0 1 1 0 0;
0  0  0  0 0 0 0 0 1 1 0 1  : 0 0 1 1 0 1;
0  0  0  0 0 0 0 0 1 1 1 0  : 0 0 1 1 1 0;
0  0  0  0 0 0 0 1 1 1 1 0  : 0 0 1 1 1 1;
0  0  0  0 0 0 1 0 1 1 1 0  : 0 1 0 0 0 0;
0  0  0  0 0 0 1 1 1 1 1 0  : 0 1 0 0 0 1;
0  0  0  0 0 1 0 0 1 1 1 0  : 0 1 0 0 1 0;
0  0  0  0 0 1 0 1 1 1 1 0  : 0 1 0 0 1 1;
0  0  0  0 0 1 1 0 1 1 1 0  : 0 1 0 1 0 0;
0  0  0  0 0 1 1 1 1 1 1 0  : 0 1 0 1 0 1;
0  0  0  0 1 0 0 0 1 1 1 0  : 0 1 0 1 1 0;
0  0  0  0 1 0 0 1 1 1 1 0  : 0 1 0 1 1 1;
0  0  0  0 1 0 1 0 1 1 1 0  : 0 1 1 0 0 0;
0  0  0  0 1 0 1 1 1 1 1 0  : 0 1 1 0 0 1;
0  0  0  0 1 1 0 0 1 1 1 0  : 0 1 1 0 1 0;
0  0  0  0 1 1 0 1 1 1 1 0  : 0 1 1 0 1 1;
0  0  0  0 1 1 1 0 1 1 1 0  : 0 1 1 1 0 0;
0  0  0  1 1 1 1 0 1 1 1 0  : 0 1 1 1 0 1;
0  0  1  0 1 1 1 0 1 1 1 0  : 0 1 1 1 1 0;
0  0  1  1 1 1 1 0 1 1 1 0  : 0 1 1 1 1 1;
0  1  0  0 1 1 1 0 1 1 1 0  : 1 0 0 0 0 0;
0  1  0  1 1 1 1 0 1 1 1 0  : 1 0 0 0 0 1;
0  1  1  0 1 1 1 0 1 1 1 0  : 1 0 0 0 1 0;
0  1  1  1 1 1 1 0 1 1 1 0  : 1 0 0 0 1 1;
1  0  0  0 1 1 1 0 1 1 1 0  : 1 0 0 1 0 0;
1  0  0  1 1 1 1 0 1 1 1 0  : 1 0 0 1 0 1;
1  0  1  0 1 1 1 0 1 1 1 0  : 1 0 0 1 1 0;
1  0  1  1 1 1 1 0 1 1 1 0  : 1 0 0 1 1 1;
1  1  0  0 1 1 1 0 1 1 1 0  : 1 0 1 0 0 0;
1  1  0  1 1 1 1 0 1 1 1 0  : 1 0 1 0 0 1;
1  1  1  0 1 1 1 0 1 1 1 0  : 1 0 1 0 1 0; /*highest state, 42*/
}/* end of file */
```

B. EPROM

The output word encoder stages of these designs required the circuit equivalent of a "look-up table" for mapping of the cyclical output of the priority encoders to an output word or state. This function was accomplished via using the address lines of the EPROM as the input function with the logical state of that combination held in the address location. As in the case of the GAL components, the capability to alter the programming of the device was a key to the selection of the EPROM for this application. One negative aspect of the EPROM selection however was an order of magnitude difference in propagation delay between the two families of devices (120 vs 15 nanoseconds, EPROM and GAL respectively).

Programming of the EPROM was significantly different from the GAL. Typically an EPROM contains source code for a microprocessor type of application. This code would be compiled from a language such as C then converted to a binary form and then loaded via an programming unit. In this case a text file of the mapping from address to output word was generated via a text editor. This file was then converted to binary via a software utility (HEX2BIN) and loaded into the EPROM on a PC based programmer. Abbreviated segments of this coding scheme with comments is shown below. Note for reference purposes that this code is in the Tektronics format, comments are in italics, spaces are for clarity and both are not part of the original data file.

```
BEGINNING OF FILE
Col 1:  / required by format
Col 2 - 5:  hex address
Col 6-7:  required by format
Col 8-11: data (output word)
/ 0000 01 0000         FIRST  WORD
/ 0111 01 0001
/ 0222 01 0002
/ 0332 01 0003
/ 0431 01 0004
/ 0420 01 0005
/ 0310 01 0006
/ 0201 01 0007
/ 0102 01 0008
/ 0012 01 0009
/ 0021 01 000A
/ 0130 01 000B
/ 0230 01 000C
/ 0321 01 000D
/ 0412 01 000E
/ 0402 01 000F
/ 0301 01 0010
/ 0210 01 0011
/ 0120 01 0012
/ 0031 01 0013
/ 0032 01 0014
/ 0122 01 0015
/ 0211 01 0016
/ 0300 01 0017
/ 0400 01 0018
/ 0411 01 0019
/ 0322 01 001A
/ 0232 01 001B
/ 0131 01 001C
/ 0020 01 001D
/ 0011 01 001E
/ 0102 01 001F
/00000000      FILE TERMINATION WORD
```

APPENDIX B. SYSTEM ASSEMBLY AND CALIBRATION

This section details the alignment and routine procedures necessary to operate the electrooptic analog to digital converter as described in the main body of the thesis. The goal was to provide a repeatable procedure for future developmental efforts; therefore extensive comments are provided. A summary of equipment used is included as Table 4.

A. OPTICAL SYSTEM

The optical bench designed for this project was described by Crowe (1995) and modifications were described in Chapter V, section B. Details of the critical connections are described by section.

1. Pulse generation

The reference pulse used by the system is generated by a Hewlett-Packard HP-71600B G bit/s Error Test Set. As the nomenclature states this is a high data rate test set intended to be used in a closed loop fashion with a data link. To perform these tests at gigabit rates the test set must have very low data pulse jitter tolerance. This is also a key requirement for the laser pulses in a sampling function.

For laser pulse generation the data output of the test set can be routed to the optical bench laser directly or via a fiber optic transmitter/receiver pair, (see Figure 32). Note, all of the electrical connections in the data path are ECL and should be terminated with 50 Ω loads during measurements. A typical user configuration of the HP-71600 is shown in Figure 33. This pattern was stored in the mass storage unit as "User Pattern 6," the key parameters are the output clock rate, data length and bit value (0 or 1). As an example, for a 40 nanosecond pulse duration with 200 nanosecond pulse repetition interval the following values would be programmed via the user soft key menu:

output clock frequency: 100 MHz (or 10 nanoseconds per bit)

data length: 20

data: 1111 0000 0000 0000 0000

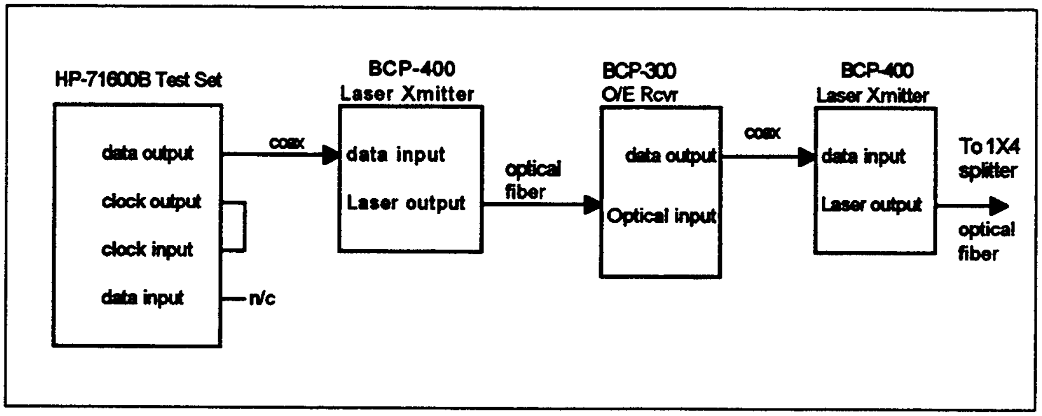
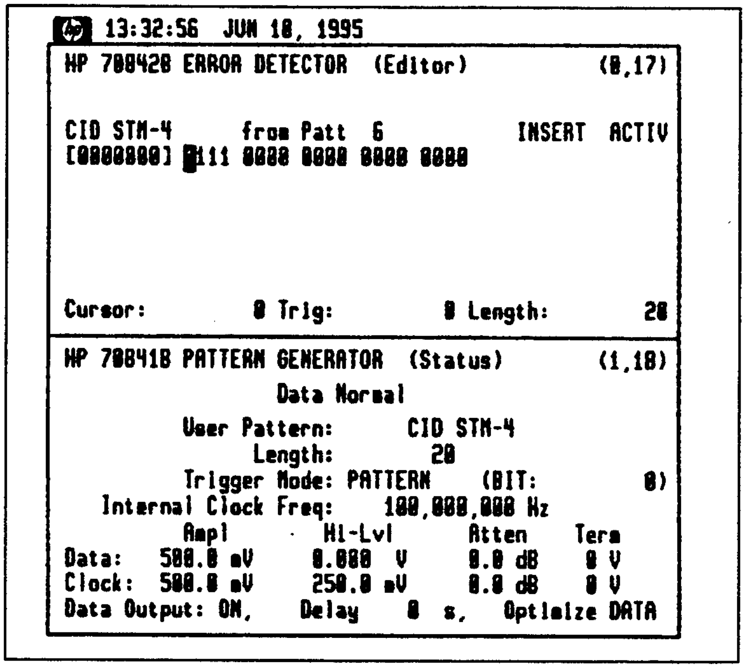


Figure 32. Laser Pulse Generation Method



```
13:32:56  JUN 10, 1995
HP 70842B ERROR DETECTOR  (Editor)              (0,17)

CID STM-4       from Patt  6             INSERT  ACTIV
[00000000] 0111 0000 0000 0000 0000





Cursor:           0 Trig:          0 Length:        20
HP 70841B PATTERN GENERATOR  (Status)           (1,10)
                 Data Normal
         User Pattern:      CID STM-4
              Length:         20
         Trigger Mode: PATTERN     (BIT:            0)
   Internal Clock Freq:    100,000,000 Hz
         Ampl         Hi-Lvl       Atten     Term
Data:    500.0 mV     0.000  V     0.0 dB     0 V
Clock:   500.0 mV     250.0 mV     0.0 dB     0 V
Data Output: ON,    Delay    0  s,   Optimize DATA
```

Figure 33. Data Screen From HP-71600 Bit Error Test Set

Regardless of how the pulse trigger was generated, the final stage was the laser pulse from the BCP-400 laser transmitter. This was a commercial grade data transmitter capable of gigabit rates with a polarized laser diode output (note: BCP Corp. does not specify a connector keying for this polarization, it was a benefit of their design not an intentional feature). The laser is connected to the pulse trigger source via the digital input (ECL), select "digital" on the front panel input selector switch, a 50 Ω termination should be placed on unused analog input, bias calibrated mode via rear panel switch, and adjustment of the threshold potentiometer to the desired pulse width. When it is desired to use the laser in a continuous mode disconnect the trigger source from the digital input and the laser will operate at 50% of maximum power. Caution is advised when operating this laser source, read the warning labels.

2. Fiber Considerations

Mach-Zehnder interferometers are phase modulation devices by design. As such, they require a polarized input for proper operation. The interferometers used in this project were fabricated with polarization maintaining (PM) optical fiber cable for inputs and single mode (SM) fiber for output. FC type connectors were used extensively on the interferometers, however one used a Radiall VFO connector for input. Reference Figure 18 for connectors used in this version of the optical bench. This combination of PM fiber and a variety of connectors presented a challenge.

The solution to the PM fiber issue was resolved by using short lengths of SM fiber as the interconnects and securing the fiber to the bench to avoid polarization rotation effects caused by microbending of the fiber. This solution was feasible for the lab environment but it did require careful adjustment of the fiber physical arrangement for even optical power distribution. A single mode 1 X 4 splitter was used as well. Special FC-FC panel mount connectors were used for coupling the fibers terminated with FC connectors. These connectors allowed rotation of the fiber connectors vice the normal keyed panel mounts, thus allowing for polarization adjustments. Optical gel was used on all panel mount coupled joints to reduce losses, this gel should not be used on the active instrument areas of the optical circuit (i.e. BCP 400 or BCP-310).

The output of the interferometers used SM fiber with SM-ST panel mounts. This allowed for additional fiber lengths to act as delay lines adjusting for path length differences, as discussed in Chapter V, section B.1.c. Finally, the BCP-310 receivers were terminated with ST connectors.

B. ELECTRICAL SYSTEM

1. Input Signal Attenuation

Input to the interferometers must be amplified for the minimum modulus and subsequently scaled for the remaining moduli. This scaling procedure was referred to as attenuation in this procedure. In addition, a DC bias signal (three independently variable signals in this project) was summed with the input to each interferometer to alter the respective operating points. For the purpose of this description the standard input source will be a Hewlett-Packard model HP-3312 function generator. The reference device for these measurements has been a multichannel digital storage oscilloscope, a Tektronics TDS-420 for example, see Figure 34 for test configuration.

The attenuation and DC bias adjustments are performed while the laser is in a continuous wave vice pulsed mode and the electrical source for these tests should be a ramped voltage from the intended maximum negative to maximum positive input voltage for a given dynamic range. A triangular waveform or a triangular wave with skewed symmetry have been used extensively for this purpose. Be aware when comparing the input to output that the op amps used for the input gain were configured in an inverting mode.

Finally, note that electrical input of the interferometer should not exceed the V_{max} of the interferometer. Exceeding this value may result in catastrophic damage to the interferometer.

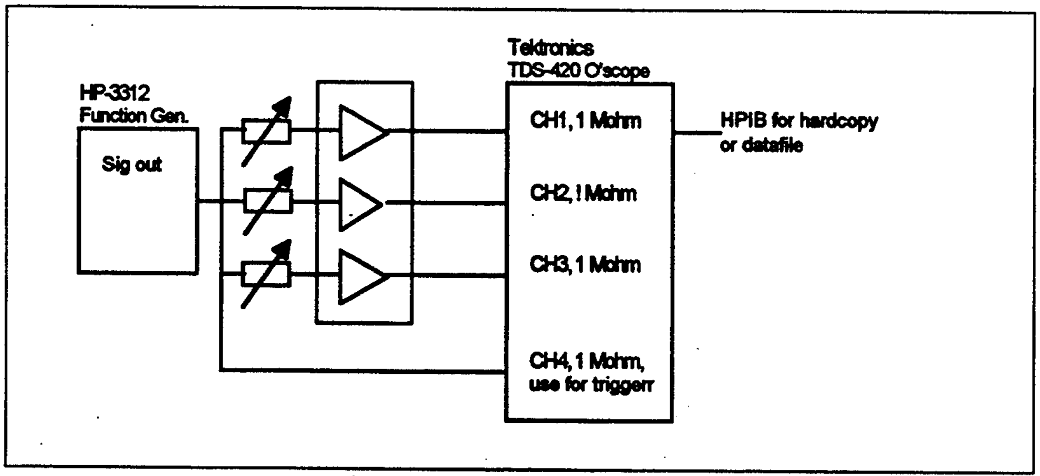


Figure 34. Gain Stage Testing

a. Gain Stage/Attenuation Initial Alignment

The first step in the attenuation alignment was to establish the gain of the minimum modulus without an interferometer connected (as a protective measure for the interferometer) and with the DC bias circuit disconnected. This step is used to determine if the voltage gain required by design calculations could be achieved. In the 5 bit case, a 10 kHz triangular wave was applied to the input of the gain stage while the oscilloscope monitored the input and output (1 MΩ input load on TDS-420). For this circuit a gain factor of approx. 20.5 was used with no subjective distortion of the waveform. The gain stages for the other moduli were then adjusted to this gain factor as a starting point for further alignment.

b. Interferometer Connection and Oscilloscope Configuration

At this point the interferometer electrical inputs were connected to the gain stages, the laser was set up for continuos output, the interferometer outputs were routed through the BCP-310 receivers and then amplified again by the HP-8347A wideband amplifiers (the automatic level control should be disabled for this application). The HP-8347 outputs were routed to the TDS-420 inputs, modulus 3 to CH1, 4 to CH2, 5 to CH3, and the output of the signal generator was "T" connected to CH4. The TDS-420 was set to 50 Ω loads for CH1-3 and 1 MΩ for CH4. If the gain stages are adjusted for equal amplitude at this point, the folding waveforms on the TDS-420 should show a roughly equivalent periodicity for all three moduli.

c. Folding Period Adjustment

Now the folding period of a segment of the lowest moduli (e.g. modulus 3) was needed for a reference, so one or two folds were measured and a reference period was calculated for one fold. Multiple folds could be measured for greater accuracy if desired. The folding period for the other moduli, T_m, can then be calculated by multiplying the reference period, T_{ref}, by a factor of the desired moduli divided by the reference moduli or

$$T_m = T_{ref} \times (\frac{m}{m_{ref}}) \tag{18}$$

As an example, suppose the folding period of the reference moduli (moduli 3, for example) as shown in Figure 35 was 10 usec (using the center graticule as the reference, trace 1 is modulus 3, etc.) and the desired moduli was 4. The desired period for modulus 4 would be 10 usec multiplied by 4/3 or 13.33 usec. The gain of this stage (modulus 4) would then be adjusted for this folding period by means of the potentiometer shown in Figure 11 for modulus 4. This process would be repeated for modulus 5. Note if it is found that the alignment cannot be performed accurately with equal resistance values for the potentiometers shown in Figure 11, then the potentiometer resistance values should be increased until a near mid-range value can be used for this adjustment. This was done for the values used in Figure 11 and the results were 10 k, 100 k, and 100 kΩ potentiometers.

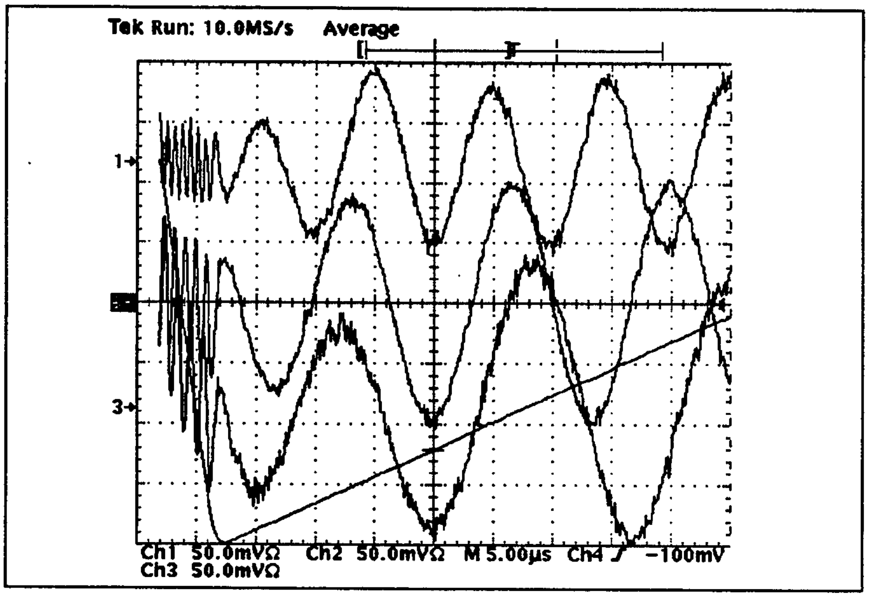


Figure 35. Attenuation Adjustment Example

2. DC Bias Adjustment

The function of DC bias in this system is to allow for shifting of the MZI operating points to allow for a voltage synchronized starting point for all moduli. This was required due to the modification of the folding period by attenuation and minor variations in the MZI operating points. As shown in Figure 36, and as would be expected of differing moduli, adjustment in bias will be needed to create a point of mutual extinction of the waveforms which will define the initial state.

The method chosen was to overlay the input ramp and find the negative voltage point (input voltage shown on the figures) of the dynamic range. This should be the one point where the waveforms are in phase. The ultimate goal of the DC bias application is to align this instance of synchronization across the input voltage range and use this point as the lowest state for encoding the output word. This point can be calculated from the number of folds required in the system, Equation 14, multiplied by the V_π for the interferometer. For example, if 5.1 folds were required and the V_π value was 2.2, then most negative point will be at 11.4 volts applied to the minimum modulus interferometer.

Since the input prior to the gain stage is displayed vice the voltage applied to the interferometer, the voltage reference must be calculated prior to the gain stage. For example, if the gain stage for modulus 3 was 20.5 then the voltage applied to achieve -11.4 volts would be .554 volts.

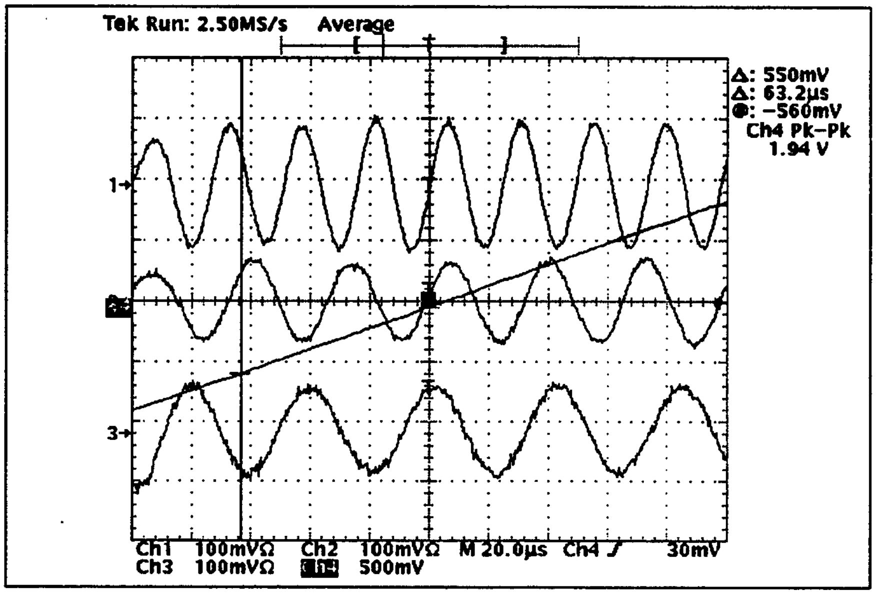


Figure 36. Folded Waveform Prior to Alignment

The most efficient method found for this alignment was to extend the operating region of the MZI system beyond the desired maximum input range a small number of folds then align the existing folds at the desired maximum negative value. The system and TDS-420 were set up as in the previous attenuation alignment The DC bias circuit would then be set to a null value of approx. 0 volts on each output, reference Figure 11. With the system power off, the DC circuit should now be connected to the inverting inputs of the respective op amps and power applied to the system.

A typical alignment is shown as Figure 37, note the cursor position on the left side of the display. The recommended procedure would be:

(1) Select the paired cursor mode on the TDS-420, Channel 4 (input voltage).

(2) Position the right cursor at the zero crossing.

(3) Move the left cursor to the desired operating point along the CH4 waveform. Note the voltage is displayed on the upper right corner as a Δ:..mV.

(4) This is the initial state alignment point.

(5) Adjust the DC bias circuit until the folding waveforms align as shown in Figure 37.

(6) The volts per division may be expanded for greater accuracy.

A fine adjustment of this value can also be performed after the initial adjustment by using the system in the pulsed mode. This method uses a DC source to present the most negative input voltage to the electrical system and monitoring the pulsed output of the interferometers. The initial point occurs when the three moduli are at a minimum intensity level.

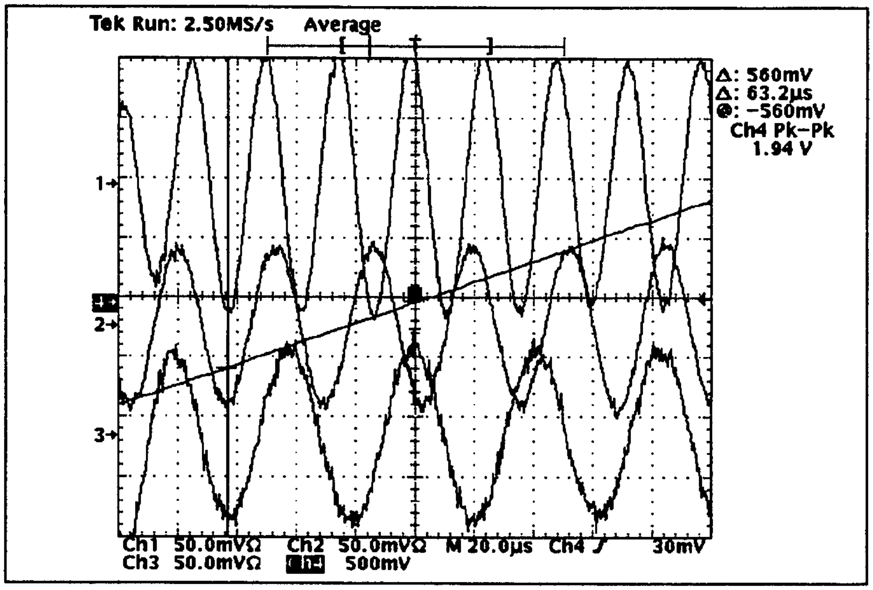


Figure 37. Folded Waveform After Alignment

c. Photodetector Gain

The final adjustment required in the analog signal path was the BCP-310 photodetector gain, see Figure 10. This provided a means to compensate for variations in maximum pulse height due to factors such as optical path loss differences or amplitude changes from intentional variations in the duty cycle. It should be noted as well that this is the only point to vary the gain of the analog signal after conversion from optical to electrical (i.e. all subsequent gain stages were fixed magnitude). The system is assembled into a complete form at this point of the test.

This procedure is based on application of a DC level to the interferometer signal input and adjustment of this value to achieve a maximum pulse height (adjusting each moduli independently) measured at the respective moduli comparator circuit input (a 10X probe was used to limit circuit interaction). The TTL output of the comparator bank is monitored while the gain is adjusted until all comparators within the bank are firing but not excessively over driven. While this is a subjective measurement of the level of over drive, experience with the comparators used in the design will indicate when the devices are driven beyond a functional state. This method was the only alignment developed due to the bipolar nature of the pulse after the amplification stages. A more empirical method could be developed if the pulses were clamped to a zero reference.

2. Circuit Card Adjustment

The only variable components on the circuit card are the voltage threshold adjustments. These values were calculated via software written by Yamakoshi (1995) as normalized values. The actual value was found by multiplying the normalized value by the desired voltage reference. This is shown in the main text as Table 2. A 10-20 mV tolerance was allowed on these values due to practical measurement/potentiometer limitations. A Fluke 8840 DMM with four digit accuracy was the standard measurement device.

3. Post Circuit Card Processing

All down stream processing of the data generated by the encoding circuitry was analyzed by a Hewlett-Packard HP 16500 logic analyzer, see Figure 38. The analyzer had the capability to establish two "machines" or process paths for data. This was convenient to look at timing functions such as comparator outputs while having a simultaneous view of the output states from the encoder circuitry. The chart format was used most often for state analysis and is shown extensively in the main text. This mode converted the output word into a user selected format (decimal was chosen for convenience) and charted the magnitude of the value versus a sample index. It should be noted that the state function required a clock function. A 5 MHz asynchronous clock was used for this project.

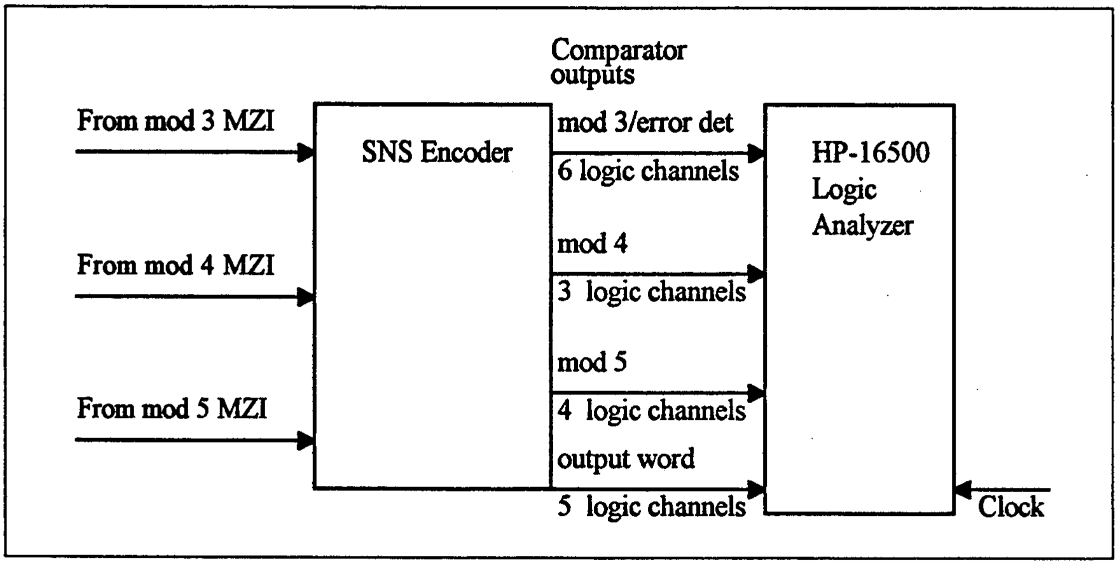


Figure 38. Logic Analyzer-SNS Encoder Configuration

Manufacturer and Part Number	Description
Hewlett-Packard HP-71600B Modules: 70841B, 70842B	Gigabit/sec. test set
Broadband Communications Products, BCP-400	Laser
Fiber Inst. Sales, 1 X 4 single mode splitter	One input, four output, single mode fiber optic splitter
Hewlett-Packard HP-3312	Function generator used as MZI input signal source
Broadband Communications Products, BCP-310	Optical/Electronic receiver
Tektronics AM501	Lab. operational amplifier
Hewlett-Packard HP-8347A	Wideband RF amplifier
Hewlett-Packard HP-16500	Logic Analyzer
Fluke 8840	Digital Multimeter
Wavetek 145	Function generator used as clock source for logic analyzer
Tektronics TDS-420	Digital Sampling Oscilloscope, 4 channel, HPIB compatible
EDC E-100C	Low impedance mVolt reference
Misc. power supplies	+5, -5.2, +/- 15 VDC

Table 4. Equipment Summary

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